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Sun Color Video Board

User's Manual

Preliminary Version 1.0
of
12th December 1982

Sun Microsystems, Inc.,
2310 Walsh Avenue
Santa Clara,
California 95051
(408) 748-9900

Revision History

Revision	Date	Comments
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Chapter 1

System Architecture

1.1. Features

- 475 by 640 pixel frame buffer
- Eight, sixteen, or twenty four color planes per pixel
- Bit map organized by (x, y) coordinates
- On-board "RasterOp" unit with 256 boolean functions
- Vector drawing speed of over 1 million pixels per second
- Region fill speed of over 5 million pixels per second
- Single board compatible with IEEE-796 Bus/Intel Multibus
- Drives any RS-170A compatible monitor with separate RGB inputs

1.2. Overview

The Sun Color Video board brings low-cost, medium-resolution bit mapped color graphics to IEEE-796/Intel Multibus based systems.

The Sun color graphics board has been specifically designed for interactive applications such as text processing, CAD, CAM, process control, and software development. Using a 'Raster-Op' function unit, the board can perform operations such as only modifying selected bit planes or XORing a new image on top of the existing image. With these features, the Sun color graphics board can rapidly display composite images, combined text and graphics, multiple character sets, variable width fonts, multiple windows, menus, icons and other symbols. In addition, the Sun color graphics board is highly suitable for applications traditionally served with vector and storage tube displays.

1.3. Introduction

The Sun Color Graphics Board controls RS-170A compatible color monitors with a horizontal line frequency of 15.75 KHz and separate inputs for sync and the red, green, and blue electron guns.

The frame buffer is configured as 512 by 640 pixel elements, but only 475 x 640 pixels are visible. For a single board configuration, the frame buffer consists of 8 planes of color so that 256 colors can be displayed simultaneously from the palette of 16 million colors. Boards can be also be stacked up to three deep, allowing images with 24 planes of color to be displayed on the color monitor. For studio applications, a future board product will allow the color board(s) to be synchronized to an externally generated RS-170 signal.

The IEEE-796 compatible color board operates at very high speeds. The board contains two sets of (x,y) registers so raster-copy or move operations can be done with a single MC68000 move instruction using pre-increment or post-decrement on the source and destination address (x/y) pointers. A single pixel update can be performed every 830 nsec, and for region-fill, 5 pixels can be written during this time frame. Thus the entire screen can be repainted in 51 msec. The board also minimizes its use of the available Multibus bandwidth by employing buffered reads and writes to perform a Multibus acknowledge within 50 nsec of any read or write request.

The board supports context switching environments. All registers, frame buffer memory, and color lookup tables can be both read and written.

The board contains four color lookup tables. These tables take the 8-bit value at each pixel location and map it into three digital 8-bit quantities specifying the intensity levels of the red, green, and blue guns on the color monitor. The use of more than one color lookup table is valuable because it allows one color lookup table to be loaded while another is being used for display; when the second table has been loaded, a single write can change the lookup table to be used for the video display, and a partially updated color lookup table will never have been used for the video display.

1.4. RasterOp Architecture

The board features a 256 function RasterOp unit operating on the eight planes at each pixel location. The RasterOp unit, described in Newman and Sproul, operates using a mask, the old frame-buffer data, the data just written to the board, and a function. The operation performed can be thought of as:

F(mask,old_data,new_data).

The mask provides for operating on an arbitrary choice of planes using one function, while operating on the other memory planes using another function For instance, the function unit can be used to quickly write character data into one bit plane while leaving the other bit planes unmodified. The function unit could also be used to XOR a symbol like a mouse on top of an existing image; when the mouse moved, another XOR would erase the mouse symbol and the process displaying the image would never be affected.

The function unit effectively off-loads the host from performing logical operations that might require up to 10 assembler instructions, and instead, reduces these operations to a single move instruction. The function unit introduces no additional cycle time to the operation of the color board.

Chapter 2

Specification Summary

Frame Buffer and Color Lookup Tables

Frame Buffer 512 x 640 x 8 pixels. Expandable to 512 x 640 x 24 by connecting three boards in parallel. Only 475 out of 512 vertical lines are visible.

Each color plane can be operated on independently of the others.

Color Lookup Table expands 8 bits of frame buffer output to 24-bits. 8-bits each for red, green, and blue monitor guns.

Four sets of red, green, and blue lookup tables. Lookup Table Set being updated can be selected independent of the set being used for video output.

Frame Buffer and Lookup Tables readable and writable.

Addressing

Device occupies 16K bytes of multibus memory space. Addressable in (x,y) coordinates.

Two sets of (x,y) registers allow separate source and destination pointers in hardware.

One x or y register can be modified in the same instruction that reads data from (or writes data to) the frame buffer.

Raster move or copy achievable in one MC68000 instruction per pixel.

Video Interface

Board drives RS-170 compatible monitors with separate red, green, blue, and sync inputs. Termination 75 ohms.

Future option will allow synchronization of board with externally generated RS-170 signal.

Nominal pixel clock 83 nsec.

Nominal horizontal frequency 15.58 khz.

Nominal vertical frequency 30 hz interlaced.

Video output settling time 5 nsec.

Update Characteristics

One frame buffer update every 830 nsec.

Update width selectable at either 1 or 5 pixels.

Entire frame buffer can be reset to background color in 51 msec.

Raster operation modifies destination data in frame buffer in conjunction with function and mask registers previously loaded.

Choice of 256 possible RasterOp operations.

IEEE-796 Bus Compatibility

D8 M20, 8-bit data only.

Either Intel or MC68000 byte-order switch selectable.

Electrical and Environmental Characteristics

+ 5.0V ± 10%. Maximum current 9.5 A. Typical current 8.0 A.

-5.2V ± 10%. Maximum current 630 mA. Typical current 600 mA.

Operating Temperature 0-60 C

Physical Characteristics

Width: 12.00 in. (30.48 cm) Height: 6.75 in. (17.15 cm) Depth: 0.50 in. (1.27 cm)

Chapter 3

Programming the Sun Color Video Board

This section provides detailed programming information about the Sun-1 color video board.

3.1. Initialization

On power-up and bus initialization, the Sun-1 color board status register is cleared. Clearing the status register disables any pending interrupts, disables the video display, exits 'paint-mode' whereby five pixels can be written in parallel, and selects color map zero for use in color map update and video refresh. No software intervention or assistance is required to complete the board initialization, although the system software may wish to set-up the default color map, clear the frame buffer, and re-enable the video display.

3.2. Frame Buffer Addressing

The color frame buffer is addressed in X and Y coordinates. One high-order bit in the address decodes whether or not to perform a read-modify-write. With this technique, random accesses to the frame buffer take two cycles; first the x (or y) offset must be set by writing a dummy datum to that address, and next, the y (or x) offset location (with the RMW address bit set) can be read or written.

Most operations on the color frame buffer, however, will take only a single 68000 instruction per pixel. Typically, a rectangle, or raster, will be operated on using the same function. Adjacent pixels are offset from each other by only a single byte in both x and y directions, so a string of pixels in the x or y-axis can be accessed merely by post-incrementing or pre-decrementing the address register pointing to the color frame buffer.

There are two sets of (X,Y) address registers on the board. The sets are selected by clearing or setting the appropriate address bit. Two sets of registers allow common raster move operations (e.g scrolling) to also be performed using one instruction per pixel.

The address registers on the board can be read for use of the board in multi-processing environments. The address registers, however, must be read-back in two stages. One read will return the low-order eight bits in the address, a second read will return the high-order bits in the address, and the software must reconstruct the full address. The reason for this interface was to keep the board usable in multibus systems with only an eight bit data bus.

3.3. Coordinate System

The frame buffer is addressed in cartesian (x,y) coordinates. The horizontal (X) axis numbers from 0 to 639. The vertical (Y) axis numbers from 0 to 511. Only vertical rows 0 to 474 are visible, and the origin of the coordinate system is located in the upper left hand corner of the screen.

3.4. Color Map Addressing

The Sun color board contains four color lookup tables. One lookup table can be used for video display while another can be selected for update by system software. The set used for video display is selected with two bits from the status register, and the set addressed on accesses to the color map is selected with another two bits from the status register.

To prevent interruption of the video image, the color map can only be updated during the vertical retrace period of the monitor. Accesses to the color map during the display period of the monitor will receive a bus acknowledge, but will not be performed. Therefore, to update the color map, software must wait for the start of a vertical retrace period. To do this, the software can use interrupts or it may poll a bit in the status register. To enable interrupts, the appropriate bit in the status register must be set, and the leading edge of the next vertical retrace period will generate an interrupt at the hard-wired interrupt level. Once the vertical retrace period has been detected, software has at most 1000 microseconds to access the color map. Periodically, the software should check that the monitor is still in vertical retrace, and, if not, the software should assume that all accesses since the previous check are invalid. Typically, in a fully loaded system, only about 600 accesses to the color map can be successfully made during a vertical retrace, so two retrace periods are normally required to load 768 entries into the color map.

Once one of the four color maps has been completely loaded with the desired data, a single write to the status register can instantly change the color map used to generate the video output.

3.5. Function Unit

The Color Graphics Board has a Function Unit for computing the pixel to write back into the display memory.

Four eight-bit registers figure in computing the Function Unit's output. These four quantities are:

- The Function
- The Source Data
- The Destination Data
- The Mask

The source data is always the data currently being written to the device, and the destination data is the data at the frame buffer location currently being accessed. Each of the mask, source, and destination registers are eight bits deep – one bit per color plane.

The function unit can be thought of as an array of eight bits. Which bit of the array is actually selected is determined by the respective values of the mask, source, and destination registers, according to the table below.

Table 3-1: Bit of Function Unit Selected as a Function of Registers

Mask	*Source*	*Destination*	*Value*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The mask, source, and destination register form a value between 0 and 7, which indexes into the eight-bit array that is the function unit. The programmer must answer the question: for this particular combination of mask, source, and destination, should the pixel at the specific addressed *x*, *y* location be a one or a zero? If the answer is yes, stick a one bit in that place in the function register; if the answer is no, stick a zero bit in that place in the function register.

Note that while each of the eight-bit mask, source, and destination registers have a bit for each color plane in the pixel, the function unit value applies to all planes in the pixel – that is, there is only a single function unit whose value applies to all eight color planes.

Table 3-2: Some Useful Raster Operations

Some Useful Raster Operations

Name	*Function Unit Value*	*Operation*
NO-OP	10101010	Dst --> Dst
INVERT	01010101	NOT Dst --> Dst
COPY	11001100	Src --> Dst
COPY INVERTED	00110011	NOT Src --> Dst
CLEAR	00000000	0 --> Dst
SET	11111111	1 --> Dst
PAINT	11101110	Src OR Dst --> Dst
PAINT INVERTED	00100010	Dst AND NOT Src --> Dst
XOR	01100110	Src XOR Dst --> Dst
WRITE MASK	11110000	Mask --> Dst
MASK OR SOURCE	11111100	Mask OR Src --> Dst
MASK XOR DESTINATION	01011010	Mask XOR Dst --> Dst

The table above showed some of the more useful RasterOp's that occur frequently. Let us work through a couple of the operations. The *COPY* operation simply transfers the source to the destination and doesn't care what the original state of the destination or mask registers is. Looking down the *Source* column, we see that the *source* field has a one in positions 2, 3, 6, and 7, and zero elsewhere. So the value that we stick in the function register is 11001100. As a second example, consider the XOR function, which is the exclusive OR of the source and destination fields. Ignoring the mask field, applying the exclusive OR function between the source and destination fields yields a one in positions 1, 2, 5, and 6, and zeros elsewhere. So the value that we stick in the function register is 01100110.

3.6. Status Register

The status register controls video enable, color lookup table selection, interrupt enable, and paint mode. The status register's bit assignments are as shown in the table below.

Table 3-3: Status Register Bit Assignments

Table 2

Status Register Bit Assignments

Bit Assignments (bit 7 = MSB)	*Function Selected on Write*	*Meaning on Read*
0-1	Selects one of four sets of color look-up tables which we can subsequently read or write. One set consists of a red, a green, and a blue color map. Updates to color map can occur only during vertical retrace on the monitor.	
2-3	Selects a set of color lookup tables through which subsequent frame buffer output will be channeled.	
4	Enable Interrupts. This bit will only generate an interrupt at the start of a vertical retrace. This bit must be cleared after an interrupt in order to clear the pending interrupt. The interrupt level is jumper selectable.	
5	Enable Paint mode. Writing to any display memory location will write five pixels instead of one. The five pixels will be horizontally adjacent to one another and start at the x-address determined by 5*(X DIV 5).	
6	Enable the color monitor display.	
7	Unused on status register writes.	On status register read, TRUE if the monitor is in vertical retrace.

3.7. Address Space Assignments

The Color Graphics Board occupies 16K bytes of Multibus memory space. The device is selected by address bits A19 through A14. Address bits A13 through A9 are used for register, color map, and frame buffer decoding; the low order address bits are used primarily for X or Y coordinate locations. All accesses to the board should be *byte* accesses.

Table 3-4: Address Space Assignments

Table 1

Address Space Assignments

Address Selection Bits								
A13	A12	A11	A10	A9	A8	A7	A6	
0	0	1	n	X	X	X	X	On read or write, update x-address register n (where n = 0 or 1) with addresses A9-A0.
0	0	0	n	X	X	X	X	On read or write, update y-address register n (where n = 0 or 1) with addresses A8-A0.
1	0	1	n	X	X	X	X	Update x-address register n (where n = 0 or 1) and New Data Register. Perform pixel read or write. Remember that on a frame buffer read request, the data received is the data requested on the previous read request.
1	0	0	n	X	X	X	X	Update y-address register n (where n = 0 or 1) and New Data Register. Perform pixel read or write.
X	1	0	X	0	0	X	X	Read or write from red color lookup table number 'N'. Set appropriate bits in status register to set 'N' where 0 <= 'N' < 4. Use address bits A7-A0 to select entry for colors 0 to 255. Operation valid only when color monitor in vertical retrace. Enable interrupts or use busy-wait read of status register to determine when monitor is doing a vertical retrace.
X	1	0	X	0	1	X	X	Read or write from green color lookup table specified by 2-bits in status register.
X	1	0	X	1	0	X	X	Read or write from blue color lookup table specified by 2-bits in status register.
X	1	1	X	0	0	0	X	Read or write status register.
X	1	1	X	0	1	0	X	Read or write mask register.
X	1	1	X	1	0	0	X	Read or write function register.
X	1	1	n	1	1	0	0	On read, read x-address register bits A7-A0 n (where n = 0 or 1) to data bus bits D7-D0.
X	1	1	n	1	1	1	0	On read, read x-address register bits A9-A8 n (where n = 0 or 1) to data bus bits D1-D0. Data bus bits D7-D2 are invalid.
X	1	1	n	1	1	0	1	On read, read y-address register bits A7-A0 n (where n = 0 or 1) to data bus bits D7-D0.
X	1	1	n	X	1	1	1	On read, read y-address register bits A9-A8 n (where n = 0 or 1) to data bus bits D1-D0. Data bus bits D7-D2 are invalid.

3.8. Multiprocessing

The Sun-1 color video board supports a multi-process environment. This allows several processes to use the board simultaneously, and hence, greatly simplifies the task of writing system software such as mouse drivers and windowing packages.

The only requirement needed in a multi-processing environment is that the state of the color board can be completely recorded by a process about to use the board, and that this state can be restored when the process is through with its timeslice. To accomplish this end, the frame buffer, the color maps, the address registers, the status register, the function register, and the mask register can all be read as well as written. This read-back capability is also attractive from the standpoint of diagnostics.

One small hitch in the read-back circuitry concerns the use of buffered reads. The last read request from the previous process will be stored in the frame buffer read latch. To restore the state of the board, the first read from the frame buffer must record this data value. By convention, this datum is written to pixel location x=639,y=511. When the current process terminates, a read from this location will restore the contents of the frame buffer read back latch. To ensure bug-free context switching, no program utilizing the non-visible portion of the frame buffer should modify this pixel location.

3.9. 24 Bit Frame Buffers

Sun Microsystems supports a configuration of three color boards connected in parallel to create a 475 x 640 x 24 frame buffer. In this configuration, each board is given a separate base address, and each board must be written to separately. RasterOps and data accesses will not operate simultaneously on the three boards, as only the sync signal and the video outputs on the boards have been synchronized. Typically the color maps in this configuration are set to achieve a 1:1 mapping between inputs and outputs, and each board drives one of the RGB electron guns on the color monitor.

For further information on this option, consult the section in this user's manual on installation and jumpering.

Chapter 4

Preparation for Use

4.1. Introduction

This chapter provides information on installing the Sun 1/4" tape interface. Included are instructions for unpacking, inspection, switch, and jumper setting, and interfacing the Sun color board with other IEEE 796-bus boards.

4.2. Unpacking Instructions

Inspect the shipping carton immediately upon receipt for evidence of damage. If the shipping carton is severely damaged, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the content and carton for the agent's inspection.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be reshipped.

4.3. Installation Considerations

The board is designed for installation into a IEEE 796-bus or Intel Multibus cardcage.

Power: The Sun color board requires both 5V and -5V power supplies. The board draws a maximum of 9.5 amps at 5V and 630 mA at -5V.

Cooling: When installing the board in an enclosed environment or under restricted airflow conditions, ensure that the internal operating temperature does not exceed 130 degrees F (55 degrees C).

Caution: To prevent possible equipment damage, do not install the board in a cardcage while power is on. Also, to prevent damage due to static voltages, avoid exposing the board to plastic materials. Finally, never insert a color board into a slot that shares a P2 connector on the multibus with another card unless that card is a properly configured color board.

4.4. Repair Information

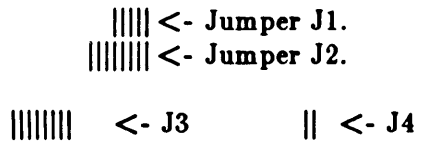
To return a Sun color board for repair, obtain a return (RMA) authorization number from the address below and send the board with the RMA number and a detailed description of the problem to the following address:

Sun Microsystems Inc
Att: Service Department
2550 Garcia Avenue,
Mountain View,
California 94043.
408-748-9900

4.5. Color Board Jumpers

First, the color board should *never* be plugged into a slot that shares a P2 connector with any other board; *unless* those other boards are *also* color boards that are configured to run in parallel with the first board.

Next, the color board has four sets of jumpers. Looking at the component side of the color board with the multibus towards yourself, they are arranged as follows:



Jumper J1 provides for connecting multiple color boards in parallel. On all standalone boards, all jumpers should be inserted.

All jumpers are left open if the board is synchronized to either an external RS170 signal (using Sun external sync board) or the board is a slave in a multiple color-board configuration.

In a multiple board configuration without an external sync board, only one color board should have J1 jumpers. In a multiple board configuration with an external sync board, no color board should have J1 jumpers.

Jumper J2 selects the base address of the device. The right-most switch is A19. The left-most switch is A12. Addresses A14 to A19 select the device. An 'O'pen switch corresponds to a zero. A closed switch corresponds to a one.

Jumper J3 selects the interrupt level. Interrupt level 7 is on the left. Interrupt level 0 is on the right. To select an interrupt level, insert a jumper at the appropriate level. Inserting no jumpers will effect a hard interrupt disable.

Jumper J4 selects between Intel and Motorola byte orders. The Sun processor uses Motorola byte order. To select Motorola byte order, insert a jumper vertically on the far right. To select Intel byte order, insert a jumper horizontally on the side closest to the Multibus. Note: one of the byte orders *must* be selected.

4.6. Coax Connectors

Each color board has four coax connectors. Viewing the card from the component side and labelling the connectors from the left, these connectors are: the external sync, red analog output, green analog output, and blue analog output. Each connector connects to a miniature coaxial cable, which in some manner must connect to a color monitor. The termination resistance on each of the inputs of the monitor should be set to 75 ohms.