SINGLE BOARD COMPUTER

SBC-200

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SECTION I

GENERAL DESCRIPTION AND CHARACTERISTICS

1.1 INTRODUCTION

The SBC-200 is a single board microcomputer designed around the powerful Z80 microprocessor. The board operates on the industry standard S-100 bus. The Single Board Computer SBC-200 is suited for data processing, industrial and process control applications (see Figure 1-1).

1.2 FEATURES

- S-100 Bus Compatible
- Z-80 Central Processing Unit
- 1024 Bytes of Random Access Memory
- 8K Bytes of EPROM using 2716
- Serial Input/Output Port (with Asynchronous and Synchronous Operation)
- Parallel Input and Output Ports
- Four Channel Counter/ Timer (Z80-CTC)
- Software Programmable Baud Rate Generator
- No Front Panel Required For Operation
- 4 Mhz Operation

1.3 SPECIFICATIONS

Board Size 5.0" x 10.0" x 0.65"

Connectors J1-S-100 Bus; J2-26 Pin J3-26 Pin

Operating Temperature

0 to 50 degrees Celsuis

Power Requirements
+8 VDC @ 1 amp (max)
+16 VDC @ 50 milliamps (max)
-16 VDC @ 50 milliamps (max)

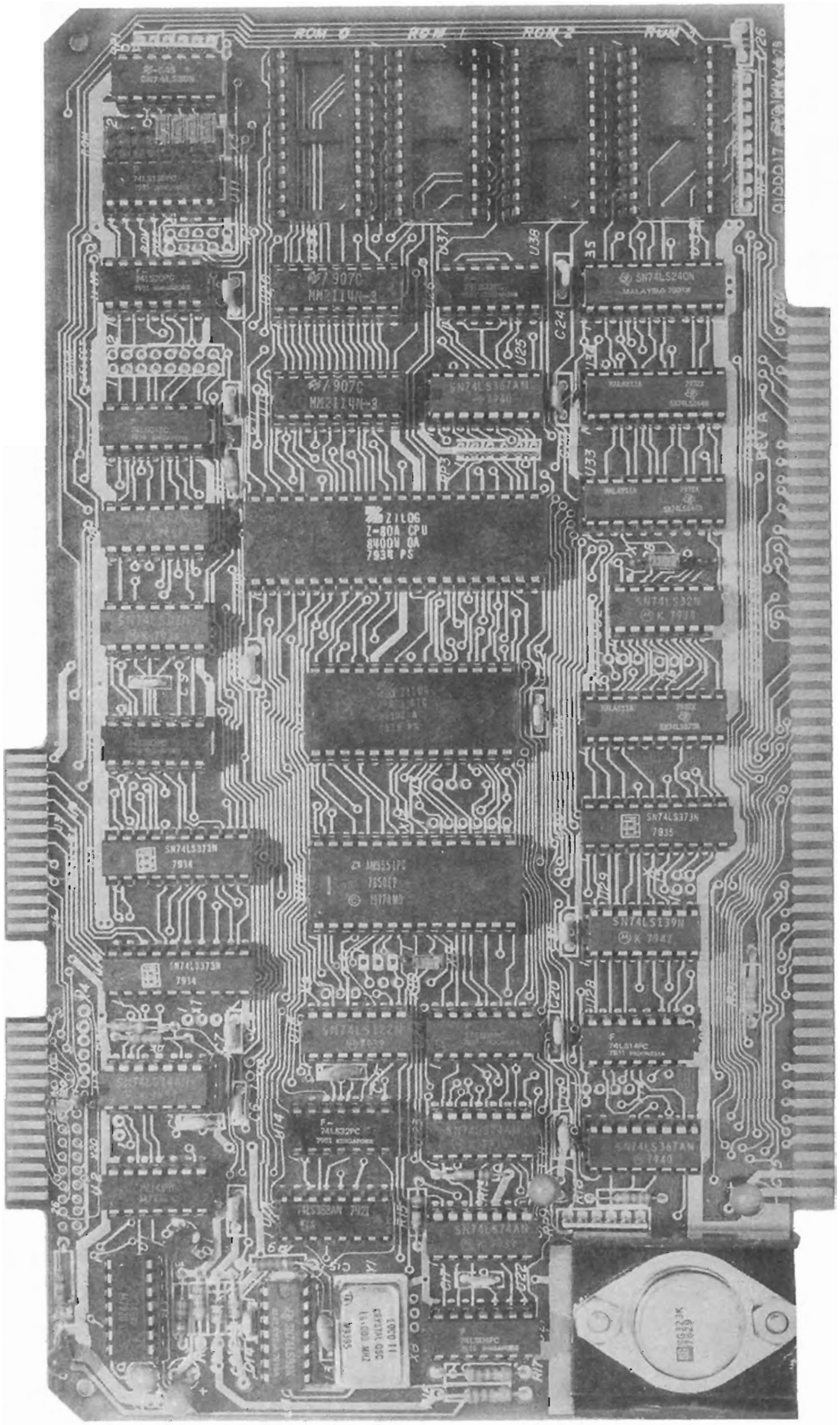


Figure 1-1. Single Board Computer SBC-200.

SECTION II

THEORY OF OPERATIONS

2.1 INTRODUCTION

This section provides a detailed analysis of the SBC-200 board. It contains:

FUNCTIONAL DESCRIPTION
SCHEMATIC DIAGRAM (Figure 2-1)
BOARD PARTS AND DESCRIPTION (Table 2-1)
CIRCUIT ANALYSIS
MEMORY
AUTO START
SERIAL INPUT/OUTPUT
PARALLEL INPUT/OUTPUT
COUNTER/TIMER CIRCUIT (CTC)
SYSTEM CLOCK OPTION
DMA OPTION

2.2 FUNCTIONAL DESCRIPTION

The SBC-200 is a Single Board Microcomputer designed around the powerful Z80 microprocessor. The Z80 microprocessor provides the major control signals required to read and write to memory and I/O ports. A 16 bit address bus and an eight bit bi-directional data bus is generated by the Z80 microprocessor.

The SBC-200 block diagram in Figure 2-1 shows the functions of the SBC-200 components. It is intended to illustrate the discussion of components and their functions in paragraphs 2.2.1 through 2.2.13.

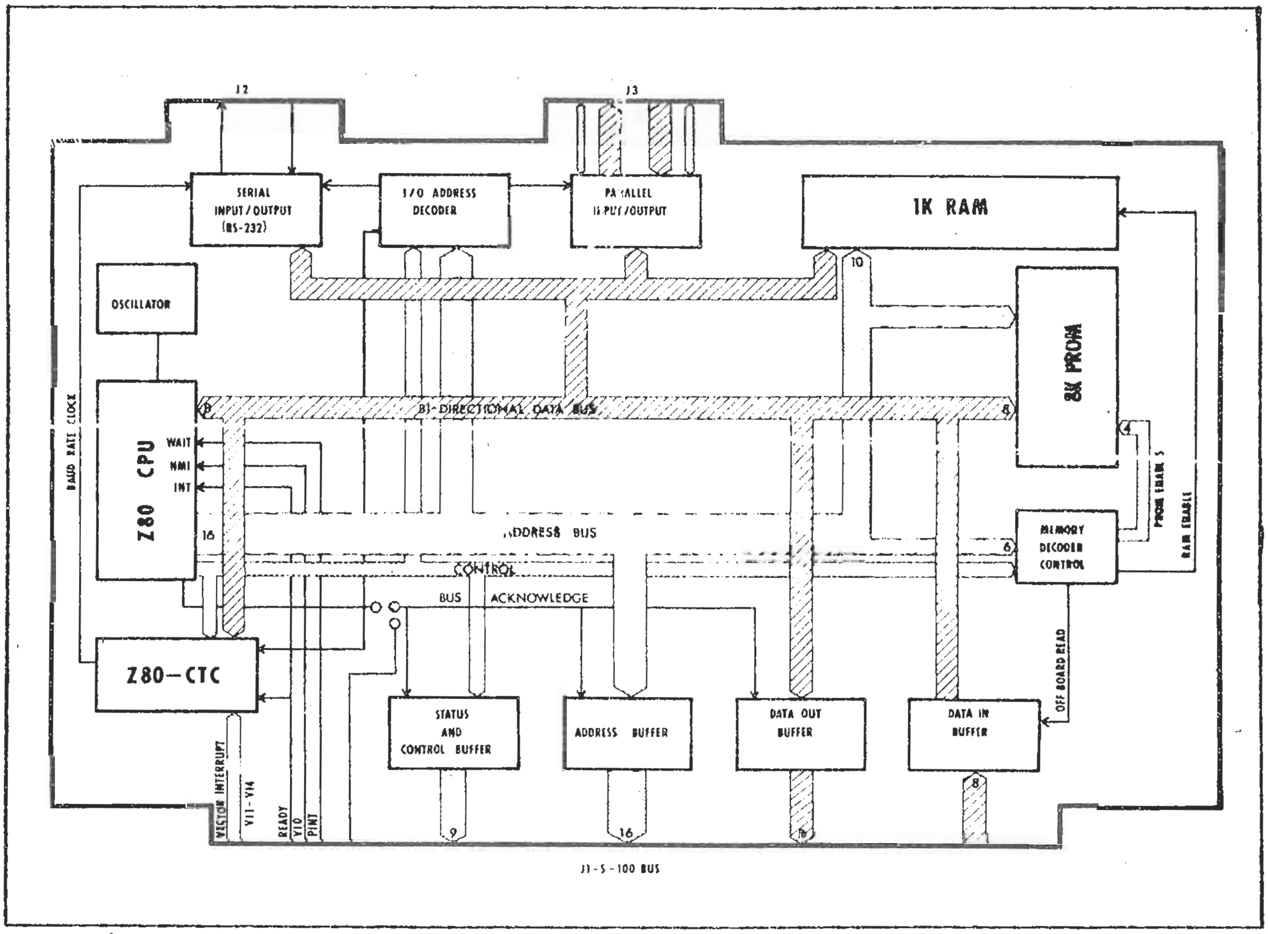


Figure 2-1. Single Board Computer SBC-200 Block Diagram.

2.2.1 Z80 CENTRAL PROCESSING UNIT

At the heart of the SBC-200 board is the powerful Z80 microprocessor chip. It provides the major control signals required to read and write to memory and input/ouput ports. The Z80 also generates a 16 bit address bus and an 8 bit bi-directional data bus.

2.2.2 CTC COUNTER/TIMER CIRCUIT

The CTC (Counter/Timer Circuit) is a circuit with four independent 16 bit counter used as "divide by" blocks for time delays event counters, or vector interrupt inputs from the S-100 bus. This permits the powerful Z80 to process in two interrupt mode. Normally, channel 0 is used for generating the 16 x baud rate clock for the serial I/O channel.

2.2.3 OSCILLATOR

A cyrstal controlled circuit used to generate the system phase clock.

2.2.4 STATUS AND CONTROL BUFFER

This component provides drive for the S-100 bus status phase clock. During a DMA1 (BUSAK=1) the status and control buffer is turned off allowing the DMA device to control the S-100 bus.

2.2.5 ADDRESS BUFFER

The address buffer is a 16 bit latch/buffer gated by MREQ=0. This buffer eliminates address changes during MREQ and turns off during BUSAK=1 (DMA).

2.2.6 DATA OUT BUFFER

This component turns on at all times except during BUSAK=1 (DMA).

2.2.7 DATA IN BUFFER

This component turns on during off board memory reading, I/O reading or interrupt acknowledge cycles to off board devices.

2.2.8 MEMORY DECODE AND CONTROL

This decoder is used for high order address bits, selecting RAM Random Access Memory, or ROM/PROM Programmable Read Only Memory which is being addressed. It also generates off-board signals used in controlling the Data-In Buffer.

2.2.9 ROM/PROM SOCKETS

These sockets accommodate up to four Read Only Memory chips or Programmable Read Only Memory chips each containing either 1K, 2K, 4K or 8K bytes of memory (total of 8K addressable).

2.2.10 RAM RANDOM ACCESS MEMORY

This component is a 1K byte status RAM Random Access Memory scratch pad, which may be strapped to occupy any area of memory.

2.2.11 PARALLEL INPUT/OUPTUT

The SBC-200 has one parallel input port and one parallel output port each having two handshake lines.

2.2.12 INPUT/OUTPUT ADDRESS DECODE

This component is a decode for the low order eight bits of address which determines the ports being accessed during input/output instructions.

2.2.13 SERIAL INPUT/OUTPUT

This component provides synchronous and asynchronous serial input/output operation via RS-232.

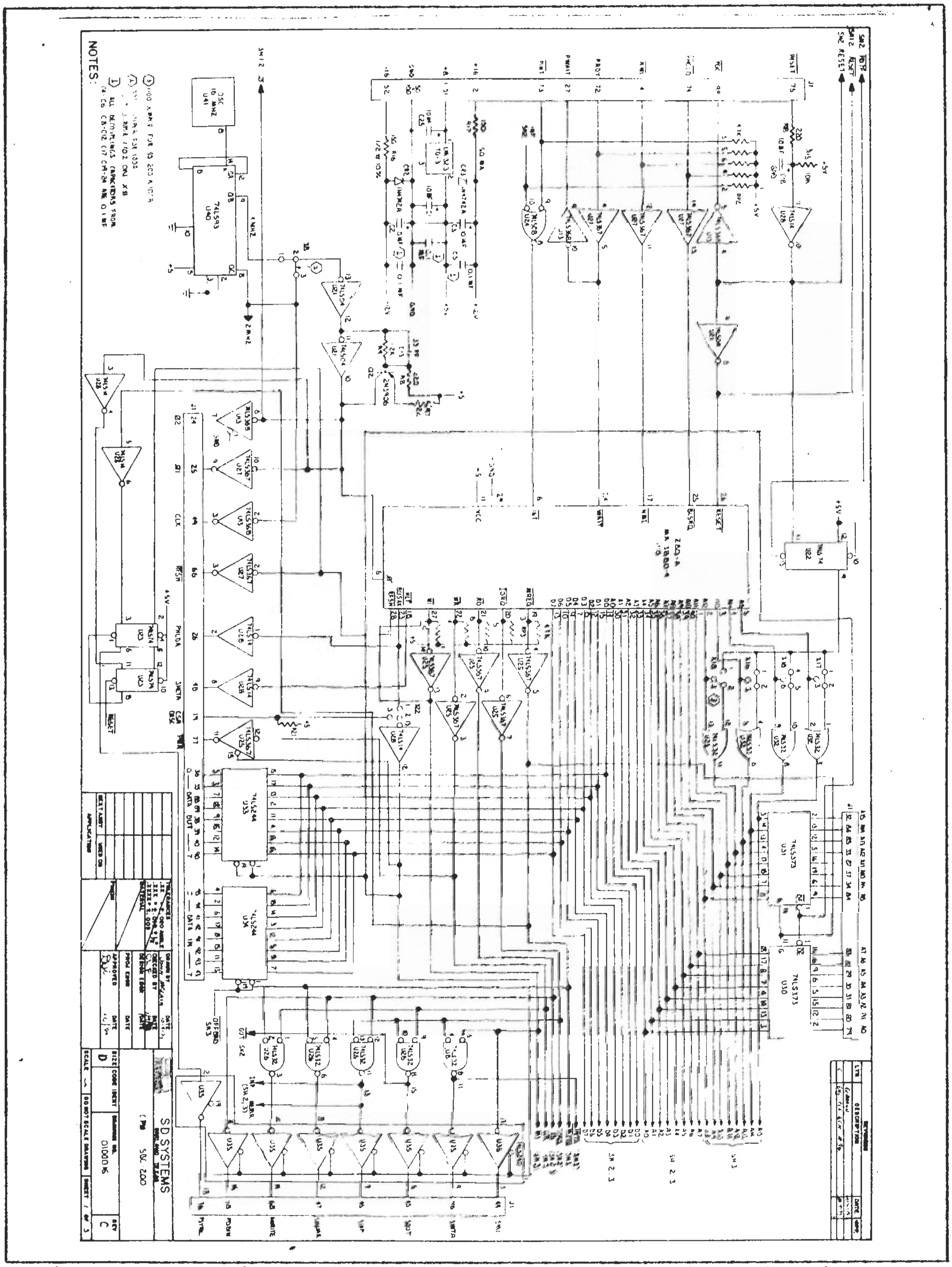


Figure 2-2. Single Board Computer SBC-200 Schematic Diagram.

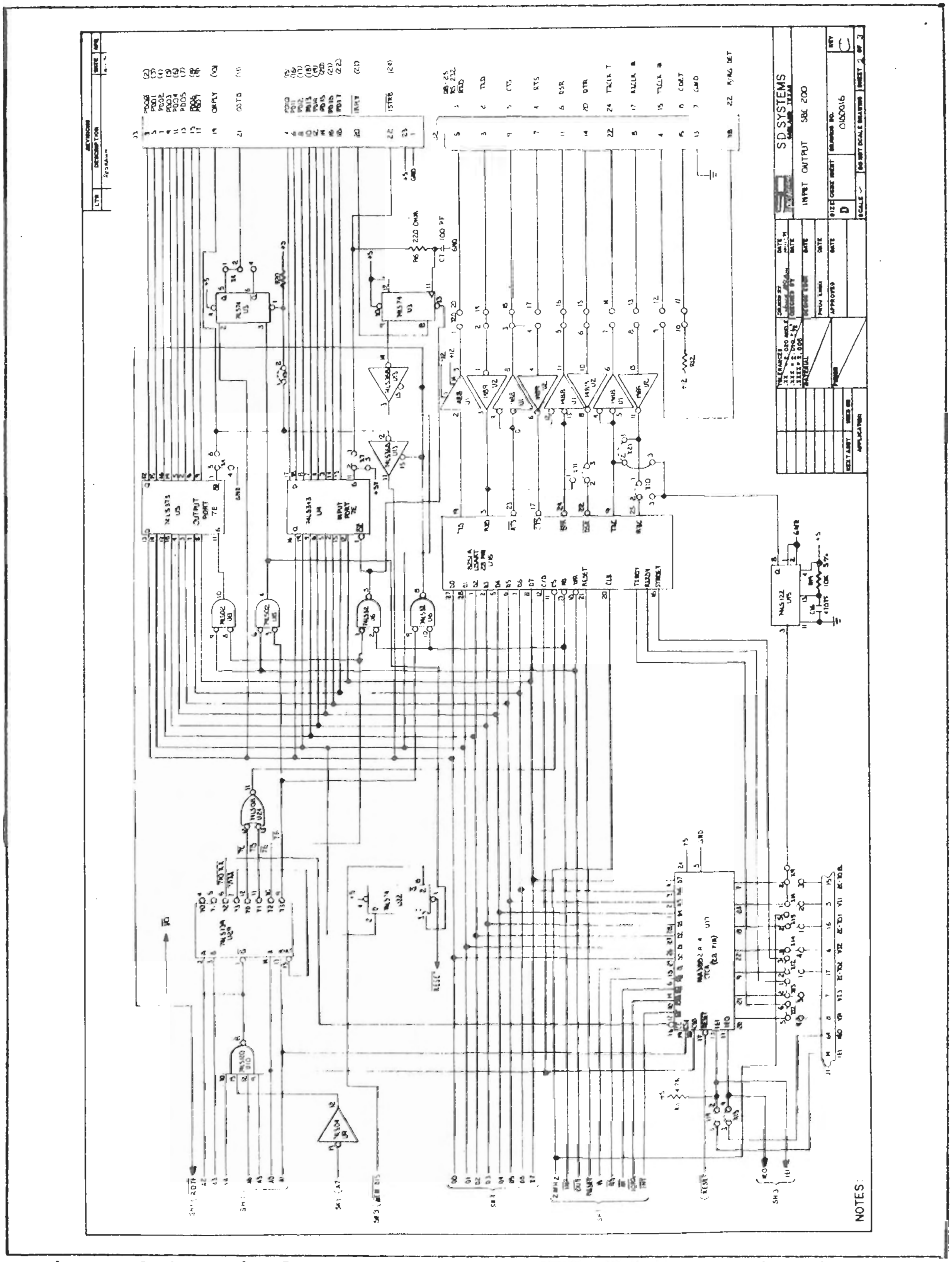


Figure 2-2. Single Board Computer SBC-200 Schematic Diagram

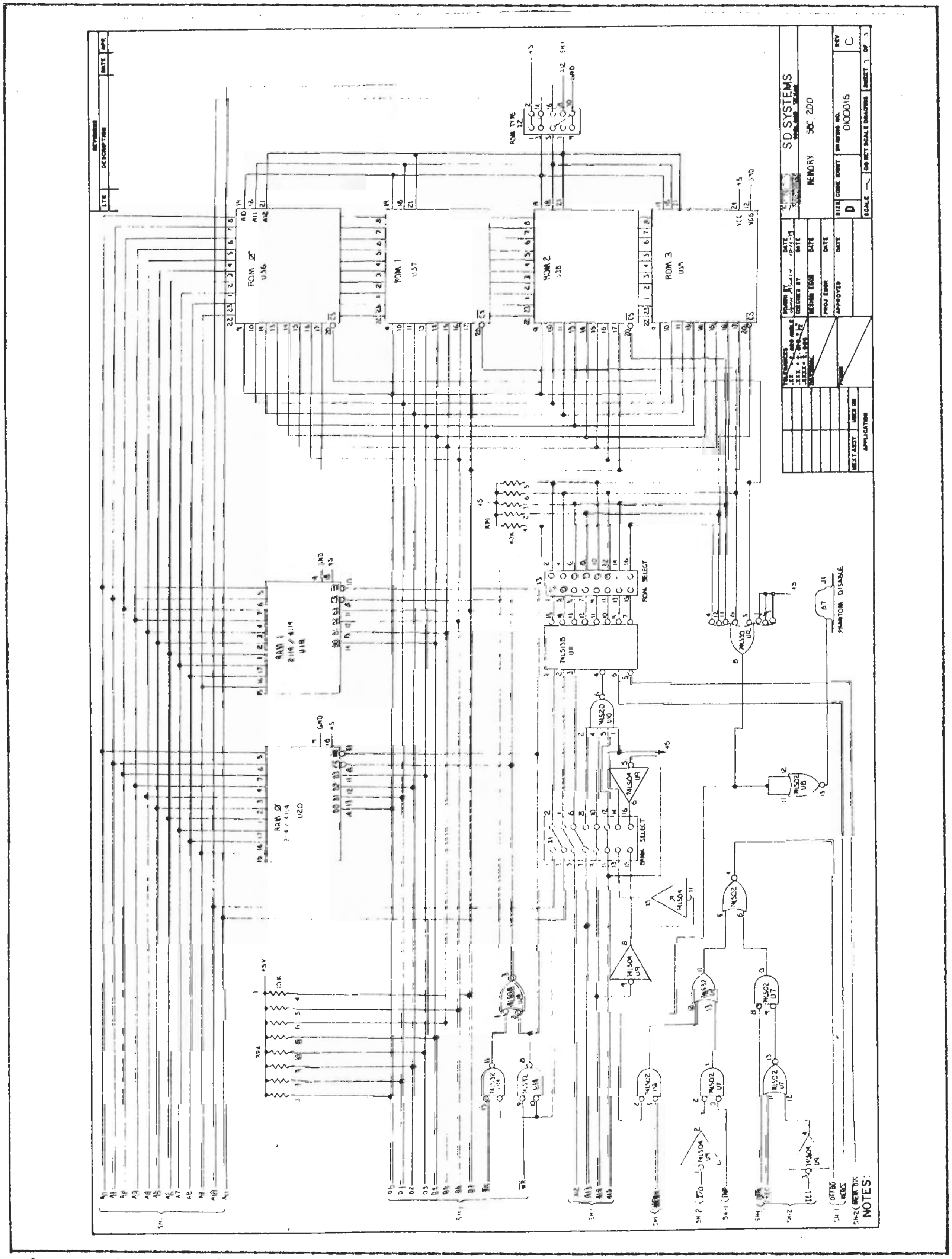


Figure 2-2. Single Board Computer SBC-200 Schematic Diagram.

Table 2-1. SBC-200 Board Parts and Description.

LOCATION	DESCRIPTION
	Information to be supplied when available.

2.3 CIRCUIT ANALYSIS

Information to be supplied when available.

2.4 MEMORY

The SBC-200 contains 1024 bytes of static RAM and sockets for 4 ROMs or PROMs. Each socket may contain a 1K, 2K, 4K or 8K byte ROM or PROM. Jumpers on the SBC-200 allow mapping the RAM and ROM to reside at any location in memory and the auto-start circuit allows reset starting on any 4K boundary. The memory on the SBC-200 takes priority over any memory on another board which might occupy the same memory addresses.

2.4.1 COMPATIBLE ROMS AND PROMS

There are a number of ROMS and PROMS which can be used in the SBC-200. The following is a list of some known compatible devices:

INTEL	2758	1K X 8 EPROM	OR EQUIVALENT
INTEL	2716	2K X 8 EPROM	"
INTEL	2732	4K X 8 EPROM	"
INTEL	2308	1K X 8 ROM	"
INTEL	2316	2K X 8 ROM	"
INTEL	2332	4K X 8 ROM	"
MOSTEK	34000	2K X 8 ROM	"
MOSTEK	32000	4K X 8 ROM	"
MOSTEK	36000	8K X 8 ROM	"
FAIRCHILD	93451	1K X 8 BIPOLAR PROM	"

2.4.2 ROM TYPE SELECTION JUMPERS

There are several jumpers which must be set up to determine the type of ROMS/PROMS to use. These jumpers are on header X2. Figure 2-3 shows the physical pin arrangement of X2.

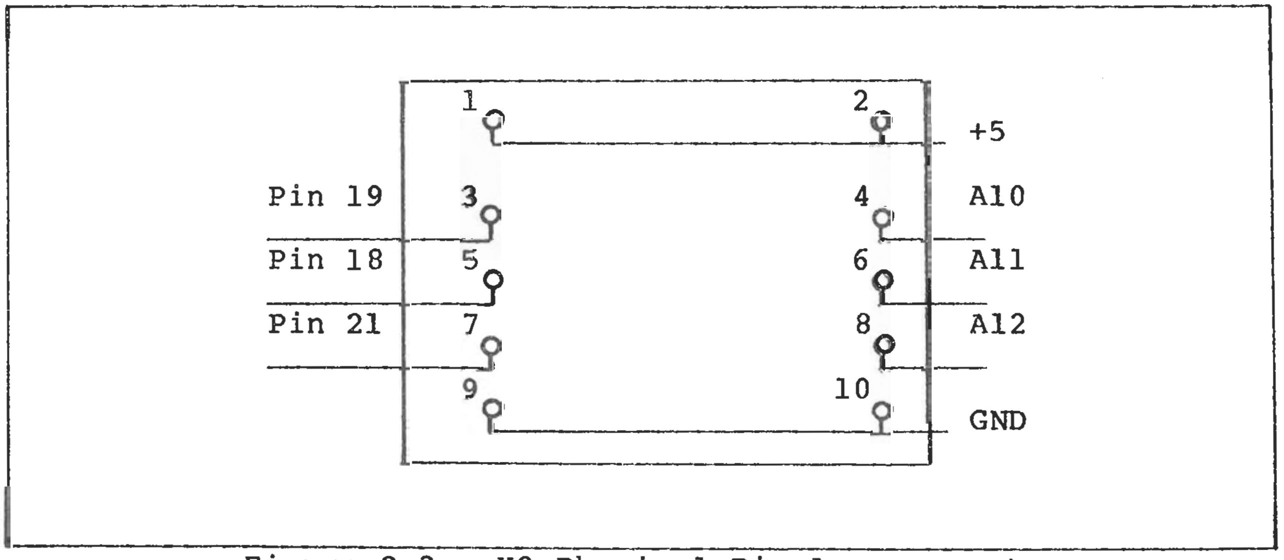


Figure 2-3. X2 Physical Pin Arrangement.

Table 2-2 contains a list of jumpers for each of the previously listed ROMS and PROMS. Note that Rev A boards are etch jumpered for 2716 EPROMS.

Table 2-2. ROMS and PROMS Jumper Listing.

PART #	DESCRIPTION	JUMPERS
I 2758	1K X 8 EPROM	X2-3,X2-9,X2-5 TO X2-10,X2-7 TO X2-1
I 2716	2K X 8 EPROM	X2-3 TO X2-4,X2-5 TO X2-10,X2-7 TO X2-
I 2732	4K X 8 EPROM	X2-3 TO X2-4,X2-5 TO X2-10,X2-7 TO X2-6
I 2308	1K X 8 ROM	SAME AS 2758
I 2316	2K X 8 ROM	SAME AS 2716
I 2332	4K X 8 ROM	SAME AS 2732
MK 34000	2K X 8 ROM	SAME AS 2716 (CUSTOM CS OPTIONS)
MK 32000	4K X 8 ROM	SAME AS 2732 (CUSTOM CS OPTIONS)
MK 36000	8K X 8 ROM	X2-3 TO X2-1,X2-5 TO X2-6,X2-7 TO X2-9
FAIRCHILD	1K X 8 BIPOLAR	X2-3 TO X2-1,X2-5 TO X2-2,X2-7 TO X2-9

2.4.3 MEMORY MAPPING

There are several selections which must be made when setting up the memory map. The first is selecting the memory bank to occupy the RAM and ROM/PROM on the SBC-200. Header X1 contains these jumpers as shown in Figure 2-4.

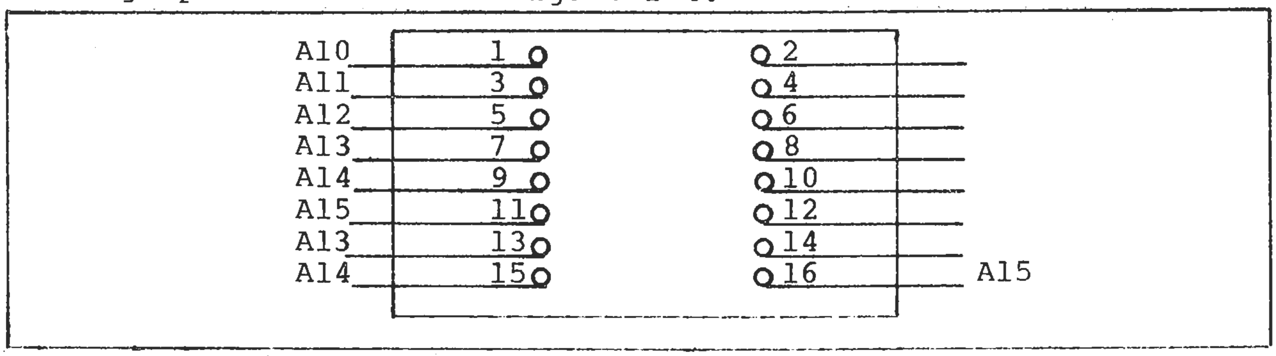


Figure 2-4. X1 Physical Pin Arrangement.

Two types of jumpers are on X1. The first type determines the number of bytes contained in each ROM/PROM socket. The second type determines the particular bank or area of the SBC-200 memory (RAM and ROM) to occupy. These jumpers are detailed in Tables 2-3 and 2-4. Revision A boards are etch-jumpered for 2K Byte ROMS to reside in the top (Bank #3) of memory.

Table 2-3. ROM Size Selection.

ROM/PROM SIZE (PER CHIP)	JUMPERS
1K BYTES	X1-1 TO X1-2, X1-3 TO X1-4, X1-5 TO X1-6
2K BYTES	X1-2 TO X1-3, X1-4 TO X1-5, X1-6 TO X1-7, X1-8 TO X1-10
4K BYTES	X1-2 TO X1-5, X1-4 TO X1-7, X1-6 TO X1-9, X1-8 TO X1-10, X1-10 TO X1-12
8K BYTES	X1-2 TO X1-7, X1-4 TO X1-9, X1-6 TO X1-11

Table 2-4. Memory Bank Selection.

ROM/PROM CHIP SIZE	JUMPERS	BANK SELECTION	BANK #
1K BYTES	X1-8 TO X1-13, X1-10 TO X1-15, X1-12 TO X1-16	0000-1FFF	0
	X1-8 TO X1-7, X1-10 TO X-15, X1-12 TO X1-16	2000-3FFF	1
	X1-8 TO X1-13, X1-10 TO X1-9, X1-12 TO X1-16	4000-5FFF	2
	X1-8 TO X1-7, X1-10 TO X1-9, X1-12 TO X1-16	6000-7FFF	3
	X1-8 TO X1-13, X1-10 TO X1-15, X1-12 TO X1-11	8000-9FFF	4
	X1-8 TO X1-7, X1-10 TO X1-15, X1-12 TO X1-11	A000-BFFF	5
	X1-8 TO X1-13, X1-10 TO X1-9, X1-12 TO X1-11	C000-DFFF	6
	X1-8 TO X1-7, X1-10 TO X1-9, X1-12 TO X1-11	E000-FFFF	7
2K BYTES	X1-10 TO X1-15, X1-12 TO X1-16	0000-3FFF	0
	X1-10 TO X1-9, X1-12 TO X1-16	4000-7FFF	1

Table 2-4. Memory Bank Selection.

ROM/PROM CHIP SIZE	JUMPERS	BANK SELECTION	BANK #
	X1-10 TO X1-15, X1-12 TO X1-11	8000-BFFF	2
	X1-9 TO X1-10, X1-11 TO X1-12	C000-FFFF	3
4K BYTES	X1-12 TO X1-16	0000-7FFF	0
	X1-12 TO X1-11	8000-FFFF	1
8K BYTES	X1-8 TO X1-10, X1-10 TO X1-12, X1-12 TO X1-14	0000-FFFF	0

Once the memory bank is selected, it is necessary to select the specific addresses each ROM/PROM socket occupies as well as the 1K bytes of RAM. Header X3 is used to select these options as shown in Figure 2-5.

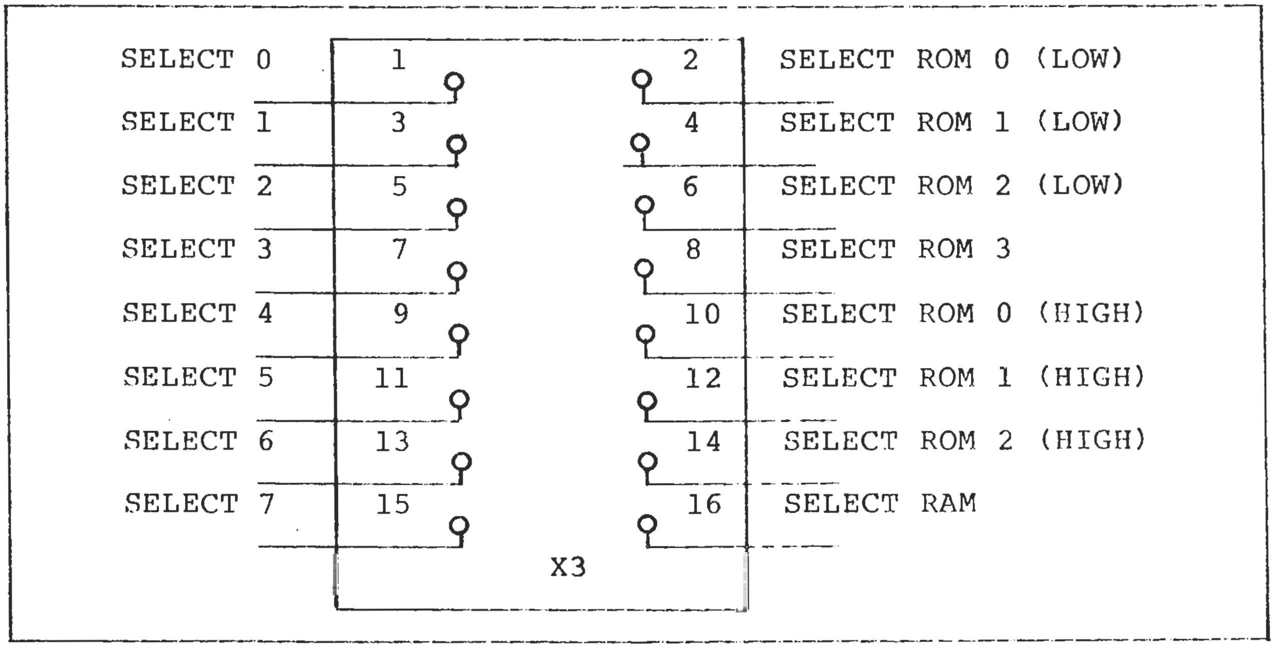


Figure 2-5. X3 Physical Pin Arrangment.

Note that ROMS 0, 1 and 2 may occupy one of two possible locations within the bank specified by the X1 jumpers in Table 2-4 while ROM 3 may occupy only one location. The RAM occupies a portion of the specified memory bank; usually the last section of a bank. Two things are important to understand at this point. First, the only sections of the memory map occupied by the SBC-

200 are those jumpered in on X3. If only one PROM is needed in the system, only install the X3 jumper for that socket. This allows use of a 64K EXPANDORAM with the SBC-200 only occupying 1K.

The second important point is when the on board 1K Static RAM is used, it occupies the same amount of memory as each of the ROM/PROM sockets (refer to Table 2-3). For example, if 2K ROM/PROMS are used, the 1K RAM occupies two contiguous 1K blocks, redundantly. Table 2-5 contains the jumpers required to select the memory space for each ROM socket and the RAM.

2.4.4 DYNAMICALLY SWITCHING OUT ON-BOARD MEMORY

All on-board memory may be switched out (disabled) of the system memory map after program control is jumped to memory on another memory board in the system. This is accomplished by the following program sequence:

```
3E  02    LD     A,2 (or 3)
D3  7F    OUT    (7FH), A   ; Switch Out SBC-200 Memory
-----------------------------------
3E  00    LD     A,0
D3  7F    OUT    (7FH), A   ; Switch In SBC-200 Memory
```

While Bit 1 of port 7F switches the SBC-200 memory in or out, Bit 0 is the handshake bit for the parallel output port. When the SBC-200 memory is switched out, a memory board in the system may occupy the same addresses space normally occupied by the on-board memory. Note that while the on-board memory is switched in, any memory writes to the 1K RAM also writes to the memory on the other board containing memory at that address. The SBC-200 always enables the on-board memory upon reset.

Table 2-5. ROM and RAM Memory Space Jumpers.

1K ROM/PROM

NAME	LOCATION	JUMPER	BANK 0	BANK 1	BANK 2	BANK 3	BANK 4	BANK 5	BANK 6	BANK 7
ROM 0	U36	X3-1 to X3-2	0000-03FF	2000-23FF	4000-43FF	6000-63FF	8000-83FF	A000-A3FF	C000-C3FF	E000-E3FF
ROM 1	U37	X3-3 to X3-4	0400-07FF	2400-27FF	4400-47FF	6400-67FF	8400-87FF	A400-A7FF	C400-C7FF	E400-E7FF
ROM 2	U38	X3-5 to X3-6	0800-0BFF	2800-2BFF	4800-4BFF	6800-6BFF	8800-8BFF	A800-ABFF	C800-CBFF	E800-EBFF
ROM 3	U39	X3-7 to X3-8	0C00-0FFF	2C00-2FFF	4C00-4FFF	6C00-6FFF	8C00-8FFF	AC00-AFFF	CC00-CFFF	EC00-EFFF
ROM 0	U36	X3-9 to X3-10	1000-13FF	3000-33FF	5000-53FF	7000-73FF	9000-93FF	B000-B3FF	D000-D3FF	F000-F3FF
ROM 1	U37	X3-11 to X3-12	1400-17FF	3400-37FF	5400-57FF	7400-77FF	9400-97FF	B400-B7FF	D400-D7FF	F400-F7FF
ROM 2	U38	X3-13 to X3-14	1800-1BFF	3800-3BFF	5800-5BFF	7800-7BFF	9800-9BFF	B800-BBFF	D800-DBFF	F800-FBFF
RAM	U19,U20	X3-15 to X3-16	1C00-1FFF	3C00-3FFF	5C00-5FFF	7C00-7FFF	9C00-9FFF	BC00-BFFF	DC00-DFFF	FC00-FFFF

2K ROM/PROM

NAME	LOCATION	JUMPER	BANK 0	BANK 1	BANK 2	BANK 3
ROM 0	U36	X3-1 to X3-2	0000-07FF	4000-47FF	8000-87FF	C000-C7FF
ROM 1	U37	X3-3 to X3-4	0800-0FFF	4800-4FFF	8800-8FFF	C800-CFFF
ROM 2	U38	X3-5 to X3-6	1000-17FF	5000-57FF	9000-97FF	D000-D7FF
ROM 3	U39	X3-7 to X3-8	1800-1FFF	5800-5FFF	9800-9FFF	D800-DFFF
ROM 0	U36	X3-9 to X3-10	2000-27FF	6000-67FF	A000-A7FF	E000-E7FF
ROM 1	U37	X3-11 to X3-12	2800-2FFF	6800-6FFF	A800-AFFF	E800-EFFF
ROM 2	U38	X3-13 to X3-14	3000-37FF	7000-77FF	B000-B7FF	F000-F7FF
RAM	U19,U20	X3-15 to X3-16	3800-3FFF	7800-7FFF	B800-BFFF	F800-FFFF

NAME	LOCATION	JUMPER	8K ROM BANK 0	4K ROM BANK 0	4K ROM BANK 1
ROM 0	U36	X3-1 to X3-2	0000-1FFF	0000-0FFF	8000-8FFF
ROM 1	U37	X3-3 to X3-4	2000-3FFF	1000-1FFF	9000-9FFF
ROM 2	U38	X3-5 to X3-6	4000-5FFF	2000-2FFF	A000-AFFF
ROM 3	U39	X3-7 to X3-8	6000-7FFF	3000-3FFF	B000-BFFF
ROM 0	U36	X3-9 to X3-10	8000-9FFF	4000-4FFF	C000-CFFF
ROM 1	U37	X3-11 to X3-12	A000-BFFF	5000-5FFF	D000-DFFF
ROM 2	U38	X3-13 to X3-14	C000-DFFF	6000-6FFF	E000-EFFF
RAM	U19,U20	X3-15 to X3-16	E000-FFFF	7000-7FFF	F000-FFFF

2.5 AUTO START

Since many systems require RAM starting at address 0, the SBC-200 has the capability of automatically causing control to begin on any 4K boundary upon resetting the board. Table 2-6 contains the jumpers required to start on each of the possible 4K boundaries.

Table 2-6. SBC-200 RAM 4K Boundaries Jumpers.

START ADDRESS (HEX)	JUMPERS
0000	X17-2 TO X17-3, X18-5 TO X18-6, X16-2 TO X16-3, X18-2 TO X18-3
1000	X17-2 TO X17-3, X18-5 TO X18-6, X16-2 TO X16-3, X18-1 TO X18-2
2000	X17-2 TO X17-3, X18-5 TO X18-6, X16-1 TO X16-2, X18-2 TO X18-3
3000	X17-2 TO X17-3, X18-5 TO X18-6, X16-1 TO X16-2, X18-1 TO X18-2
4000	X17-2 TO X17-3, X18-4 TO X18-5, X16-2 TO X16-3, X18-2 TO X18-3
5000	X17-2 TO X17-3, X18-4 TO X18-5, X16-2 TO X16-3, X18-2 TO X18-2
6000	X17-2 TO X17-3, X18-4 TO X18-5, X16-1 TO X16-2, X18-2 TO X18-3
7000	X17-2 TO X17-3, X18-4 TO X18-5, X16-1 TO X16-2, X18-1 TO X18-2
8000	X17-1 TO X17-2, X18-5 TO X18-6, X16-2 TO X16-3, X18-2 TO X18-3
9000	X17-2 TO X17-2, X18-5 TO X18-6, X16-2 TO X16-3, X18-1 TO X18-2
A000	X17-1 TO X17-2, X18-5 TO X18-6, X16-1 TO X16-2, X18-2 TO X18-3
B000	X17-1 TO X17-2, X18-5 TO X18-6, X16-1 TO X16-2, X18-1 TO X18-2
C000	X17-1 TO X17-2, X18-4 TO X18-5, X16-2 TO X16-3, X18-2 TO X18-3
D000	X17-1 TO X17-2, X18-4 TO X18-5, X16-2 TO X16-3, X18-1 TO X18-2
E000	X17-1 TO X17-2, X18-4 TO X18-5, X16-1 TO X16-2, X18-2 TO X18-3
F000	X17-1 TO X17-2, X18-4 TO X18-5, X16-1 TO X16-2, X18-1 TO X18-2

When writing software entered upon reset, two instructions must be executed immediately following reset:

ADDRESS	SOURCE CODE	OBJECT CODE
X000	JP X003	C3 03 X0
X003	IN A,(7FH)	DB 7F

This resets the hardware which caused execution to occur at X000 instead of 0000. The only case where these instructions are not needed is when X=0 i.e. when resetting to 0000.

The SD Monitor resides at E000 and requires that the jumpers be set to cause an auto start to that address. When resetting to the disk controller prom (BIOS), set the auto start for F000.

The PC Board is etch-jumpered for auto starting at E000 or F000. Only the last jumper (X18-2) must be connected to select between the two start-up addresses.

2.6 SERIAL INPUT/OUTPUT

The SBC-200 contains one serial I/O port with an RS-232 interface. The hardware allows both asynchronous and synchronous data communications with BAUD rates from 150 to 9600. The standard SD Monitor utilizes the serial I/O port for console interaction in the asynchronous mode.

2.6.1 BAUD RATE GENERATOR

The CTC (Counter-Timer Circuit MK3880) is a four channel counter/timer and one channel is used for generating the 16X BAUD RATE CLOCK required by the SERIAL I/O.

The SD Monitor for the SBC-200 waits for the first keyboard entry after being reset, measures the pulse width of the start bit, and sets up the CTC to match the BAUD rate. Table 2-7 lists the CTC counts required for each of the standard BAUD rates from 150-9600.

Table 2-7. Baud Rate Generator.

SYSTEM CLOCK RATE	USART BY	BAUD RATE	DIVIDED BY CTC	CONSTANT	% ERROR
4.00 MHZ	64	150	208	D0H	+.16%
	64	300	104	68H	+.16%
	16	600	208	D0H	+.16%
	16	1200	104	68H	+.16%
	16	2400	52	34H	+.16%
	16	4800	26	1AH	+.16%
	16	9600	13	0DH	+.16%

2.6.2 USART

The serial communications are controlled by a 8251 USART (Universal Synchronous/Asynchronous Transmitter/Receiver). This device controls the serial to parallel to serial data conversions, synchronizing with data in both asynchronous and synchronous modes, error checking and generating the key RS-232 signals. For complete details of this device see the Intel data sheet.

The USART resides at port address 7CH AND 7DH, with 7C being data and 7D status/control.

The standard SD Monitor sets the USART up as follows:

```
LD        A, 4EH          (For 150 and 300 BAUD use 4FH)
OUT       (7DH),A
LD        A, 37H
OUT       (7DH),A
```

The baud rate is then set up by outputtting 45H following by the appropriate constant from Table 2-7 to CTC port 78H:

```
LD        A,45H
OUT       (78H),A
LD        A,13       9600 BAUD
OUT       (78H),A
```

The following routines may then be used to input and output to the serial I/O channel.

```
SERIN     IN   A, (7DH)   Input Status
          AND  2
          JP   Z,SERIN    Wait for RX data ready
          IN   A, (7CH)   Read Data
          AND  7FH        Strip off parity
          RET
SEROUT    IN   A, (7DH)   Input Status
          AND  1
          JP   Z,SEROUT   Wait for TX ready
          LD   A,C        Data in C
          OUT  (7CH,)A    Output H
          RET
```

2.6.3 SERIAL I/O CABLE

The J-2 card edge connector contains the RS-232 signals from the serial I/O port. All the signals terminate at header X20 and must be jumpered for the required systm configuration (see Table 2-8).

Table 2-8. J2 Pin-Out.

J2 PIN #	D-25 CONNECTOR (RS-232 TYPE)	RS-232 Symbol	DESCRIPTION	X20 Pin
3	2	BA	TXD	19
4	15	DB	TXCLK(M)	12
5	3	BB	RXD	20
7	4	CA	RTS	17
8	17	DD	RXCLK(M)	13
9	5	CB	CTS	18
11	6	CC	DSR	16
13	7	AB	GROUND	-
14	20	CD	DTR	15
15	8	CF	CDET	11
18	22	CE	RING INDICATE	9
22	24	DA	TXCLK (T)	14

2.6.4 SERIAL I/O JUMPER OPTIONS

Figure 2-6 illustrates X20. X20 must be jumpered for the user's system requirements and allows either modem look-alike or terminal look-alike operation. The standard option is modem look-alike which are etch jumpered on the back of the PC board. (See solid lines on Figure 2-6).

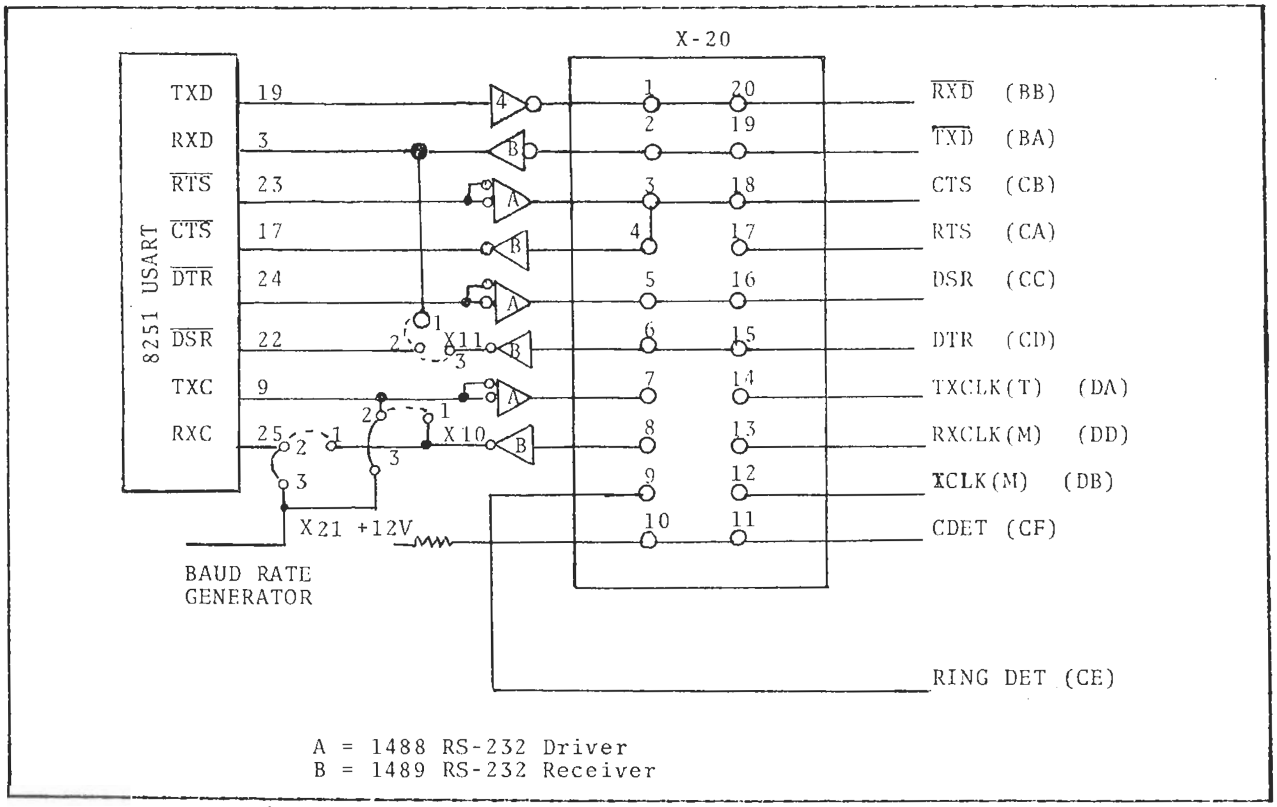


Figure 2-6. X20 Physical Pin Arrangement.

There are many possible configurations for the RS-232 interface depending upon whether the SBC-200 is to operate in "MODEM LOOK-ALIKE" or "TERMINAL LOOK-ALIKE" mode and synchronous or asynchronous mode. Synchronous modems, for example, supply the clocks for transmit and receive data (1 x BAUD RATE). In that case the RXCLK(M) and TXCLK(M) would be connected to the 8251 USART. However, the most common use of this RS-232 port is in the MODEM LOOK-ALIKE/ASYNCHRONOUS MODE. This allows direct connection to "DUMB" CRT terminals and serial printers. For other modes of operation, the user should study Figure 2-6 and make the necessary jumper connections. Table 2-9 shows the standard configuration which is etch jumpered on the back of the PC board. For other configurations these jumpers may be cut.

Table 2-9. SBC-200 Standard Configurations

FROM	TO
X20 - 1	X20 - 20
X20 - 2	X20 - 19
X20 - 3	X20 - 18
X20 - 4	X20 - 3
X20 - 5	X20 - 16
X20 - 6	X20 - 15
X20 - 10	X20 - 11
X20 - 2	X20 - 3
X21 - 2	X21 - 3

The user must connect X11 to select between using the RS-232 port for a console terminal or for a serial printer.

X11 - 1 TO X11 - 2	TERMINAL
X11 - 2 TO X11 - 3	PRINTER

X11-2 is connected to DSR on the 8251 USART. In the console terminal mode receive data (X11-1) is connected to X11-2 to allow baud rate measurement by the SD Monitor. In the printer mode DTR (X11-3) is connected to X11-3 to use as a "Printer Ready" handshake line.

2.7 PARALLEL INPUT/OUTPUT

SBC-200 contains one parallel input port and one output port with two handshake lines each. Table 2-10 contains the pin out for J3, the parallel I/O connector:

Table 2-10. J3 Pin Out.

PIN NUMBER	DIRECTION	DESCRIPTION
1		Logic Ground
3	OUTPUT	PD00, Parallel Data Out Bit 0
5	OUTPUT	PD01, Parallel Data Out Bit 1
7	OUTPUT	PD02, Parallel Data Out Bit 2
9	OUTPUT	PD03, Parallel Data Out Bit 3
11	OUTPUT	PD04, Parallel Data Out Bit 4
13	OUTPUT	PD05, Parallel Data Out Bit 5
15	OUTPUT	PD06, Parallel Data Out Bit 6
17	OUTPUT	PD07, Parallel Data Out Bit 7
19	INPUT	ORPLY, Output Reply
21	OUTPUT	OSTB, Output Strobe
23		+5 Volts
4	INPUT	PD10, Parallel Data In Bit 0
6	INPUT	PD11, Parallel Data In Bit 1
8	INPUT	PD12, Parallel Data In Bit 2
10	INPUT	PD13, Parallel Data In Bit 3
12	INPUT	PD14, Parallel Data In Bit 4
14	INPUT	PD15, Parallel Data In Bit 5
16	INPUT	PD16, Parallel Data In Bit 6
18	INPUT	PD17, Parallel Data In Bit 7
20	OUTPUT	IRPLY, Input Reply
22	INPUT	ISTRB, Input Strobe

2.7.1 PARALLEL OUTPUT PORT

The parallel output port is composed of an eight bit latch and two handshake lines. The latch is addressed at 7EH and the handshake lines at 7FH. The outputs of the latch are tri-state and may optionally be disabled by the ORPLY handshake input. The ORPLY is read via port 7FH, bit 0. This line may be used to let the SBC-200 know when the output device (such as a printer) is ready to receive data. The other handshake line (OSTB) is used to strobe the data to the output device. This line may be jumpered for positive or negative pulses and may optionally be reset by the ORPLY line. The OSTB line is controlled by a one bit latch addressed at output port 7FH, bit 0. See Table 2-11 for option selection details. Note that port 7FH, bit 1 switches the SBC-200 on-board memory in and out.

2.7.2 PARALLEL INPUT PORT

The parallel input port is composed of an 8 bit latch and two handshake lines. The 8 bit latch is addressed 7EH while the handshake lines are addressed at 7FH.

The ISTRB handshake line sets a flip-flop when a positive transition occurs. The output of this flop is read at port address 7F, bit 1, and indicates that data is available from the input device. (When bit 1=0, data is available). The flop is cleared when data is input from port 7EH. The Q of the flop is the IRPLY line which indicates to the input device that the data is received. Table 2-11 contains the details of options on the parallel input port.

Table 2-11. Parallel Input/Output Port Options.

PARAMETER	OPTIONS	JUMPERS
1. Parallel out data Enabled:	a. Always b. Only during ORPLY	X4-4 to X4-5 X4-5 to X4-6
2. Output Strobe Polarity (OSTB)	a. Positive true b. Negative true	X4-1 to X4-2 X4-2 to X4-3
3. Output Strobe Cleared by:	a. Output Reply b. Software Control	X5-1 to X5-2 None
4. Input Port Latch Gated:	a. Always b. By Input Strobe (ISTRB)	X7-2 to X7-3 X7-1 to X7-2

2.8 COUNTER/TIMER CIRCUIT (CTC)

The counter/timer circuit utilizes the MK3882-4 CTC-A chip which features four independent channels which may be configured to operate in various modes as required. See the Mostek MK3882 data sheet for details of programming the CTC-A. (Normally on the SBC-200, channel 0 is used to generate the BAUD rate clock). CTC channels 0, 1, 2 and 3 are addressed at 78H, 79H, 7A and 7BH respectively.

2.8.1 CTC AS INTERRUPT CONTROLLER

The SBC-200 allows using the CTC as a vectored interrupt controller. To do this, the channels to use as vectored interrupt inputs must be jumpered to the S-100 pins as shown in Table 2-12. Additionally, if other external interrupts must be prioritized with the CTC interrupts, pins 14 and 64 may optionally be used to create an interrupt daisy chain between boards.

Table 2-12. CTC Vectored Interrrupt Inputs.

INTERRUPT CHANNEL	SOURCE	JUMPER
0	2MHZ CLOCK VII	X14-1 TO X14-5 (STD) X14-1 TO X14-2
1	VI2 SYNDET	X14-3 TO X14-4 X14-3 TO X12-3
2	VI3 SERIAL RX READY	X13-2 TO X13-3 X13-1 TO X13-2
3	VI4 SERIAL TX READY	X12-4 TO X12-5 X12-5 TO X12-6

To use interrupt priority daisy chain, connect X19-1 to X19-2 and X15-3 to X15-4.

2.9 SYSTEM CLOCK OPTION

The SBC-200 has a standard clock rate of 4MHZ but may also be jumpered for 2MHZ (See Table 2-13).

Table 2-13. SBC-200 System Clock Jumpering.

JUMPER	0 CLOCK RATE
X8-1 to X8-2	4 MHZ*
X8-2 TO X8-3	2 MHZ

2.10 DMA OPTION

During DMA operations the data out, address, and control line drivers must be disabled. The standard configuration is with J1-19 (NEG TRUE) controlling the drivers (See Table 2-14).

Table 2-14. SBC-200 DMA Jumpering.

JUMPER	DRIVER
X22-1 to X22-2	J1-19 DISABLES DRIVER*
X22-2 to X22-3	BUSAK DISABLES DRIVER

* Standard configuration with PC board etch jumper.

SECTION III

CONSTRUCTION

3.1 INTRODUCTION

The SBC-200 kit is intended for those people who have had some prior experience with kit building and digital electronics. It is highly recommended that experienced personnel assemble and check out the board.

Appendix B shows the SBC-200 Parts List. Double check all the parts against this parts list. For proper location of parts that are to be used see Appendix C.

3.2 ASSEMBLY PROCEDURE

1. Install and solder the IC sockets in their proper location.

   14 Pin at U1-U3,U6-U10,U12,U14,U15,U21-U24,U26,U28,U32,U40
   16 Pin at U11,U13,U25,U27,U29
   18 Pin at U19,U20
   20 Pin at U4,U5,U30,U31,U33-U35
   24 Pin at U36-U39
   28 Pin at U16-U17
   40 Pin at U18

   NOTE
   Do not install a socket in location Y1.

2. Install and solder the resistors as follows:

   R6, 8, 22, 220 Ohm, 1/4W, 10% (RED,RED,BROWN)
   R12 2.4K Ohm, 1/4W, 10% (RED,YELLOW,RED)
   R7, 22 Ohm,1/4W, 10% (RED,RED,BLACK)
   R9 1.2K Ohm, 1/4W, 10% (BROWN,RED,RED)
   R11, R20, R21 4.7K, 1/4W, 10% (YELLOW,VIOLET,RED)
   R15, 19 10KOhm, 1/4W, 10% (BROWN,BLACK,ORANGE)
   R16, 17 150 Ohm, 1/2W, 10% (BROWN,GREEN,BROWN)
   RP1, 2, 3 Resistor pack 4.7K Ohm 6 Pin SIP
   RP4 Resistor pack 10K Ohm 10 Pin SIP

   NOTE
   Pin 1 of the SIP is designated by a notch or dot on the end of this package.

3. Install and solder zener diodes CR2 and CR3 1N4742A-12V with the banded end as shown on the PC board.

4. Install and solder the capacitors as follows:

C1, 2, 3, 18, 25 10MF 25V Tantalum (Note: Proper polarity)
C4-6, C8-12, 14, 15, 17, 19-24 0.1MF 50V DIP MICA
C7 100 Pf MICA
C13 33 Pf MICA
C16 470 Pf MICA

5. Install and solder the voltage regulator with the heatsink using the 6-32 hardware supplies.

   Heatsink TO-3
   VR1 323 +5V

6. Install and solder the BERG PIN HEADERS (on top side of board with long protion of Pin up).

   X3 2 BY 8
   X18 1 BY 6
   X20 1 BY 2 (Pin 1-20)
   X11 1 BY 3
   X13 1 BY 3
   X14 1 BY 4

NOTE

All X-numbers with Pin 1 are marked on the PC board. Double check all the pin headers and their pin configuration before any wire wrapping.

7. Install and solder transistor Q1.

8. Install and solder 16MHZ crystal oscillator in location Y1.

9. Double check all solder connections for cold solder joint, unsoldered connections or shorted connections.

3.3 INITIAL CHECK-OUT

Install the board into Bus-100 connector and measure the output of +5V regulator VR1, +12V and -12V of CR2 and CR3 respectively.

VR1 = +5V (Right side pin, looking from front of PCB)
CR2 = -12V (Anode)
CR3 = +12V (Cathode)

2. Measure the power supply voltages in the Single Board Computer chips. (Any of the IC sockets can be used).

NOTE

Do not proceed with board checkout until all power supply voltages are correct. The TTL and MOS logic can be permanently damaged if improper voltages are applied.

3. Install the IC's in their sockets observing the pin 1

designation on each socket marked on the PC board.

U1	75188 or MC1488
U2	75188 or MC1489
U3,22,23	74LS74
U4,5,30,31	74LS373
U16,14,26,32	74LS32
U7,8	74LS02
U9,U21	74LS04
U10	74LS20
U11	74LS138
U12	74LS30
U13	74LS368
U15	74LS122
U16	USART 8251A
U17	MK3882 A-4 CTC
U18	MK3880-4 Z804 CPU
U19,U20	2114 or 4114
U28	74LS14
U24	74LS08
U25,27	74LS367
U29	74LS139
U33,34	74LS244
U35	74LS240
U36,37,38,39	ROM 0-3 (NOT INCLUDED IN KIT)
U40	74LS93

4. Double check all IC's for proper orientation and location.

5. Install card ejectors with mounting pins.

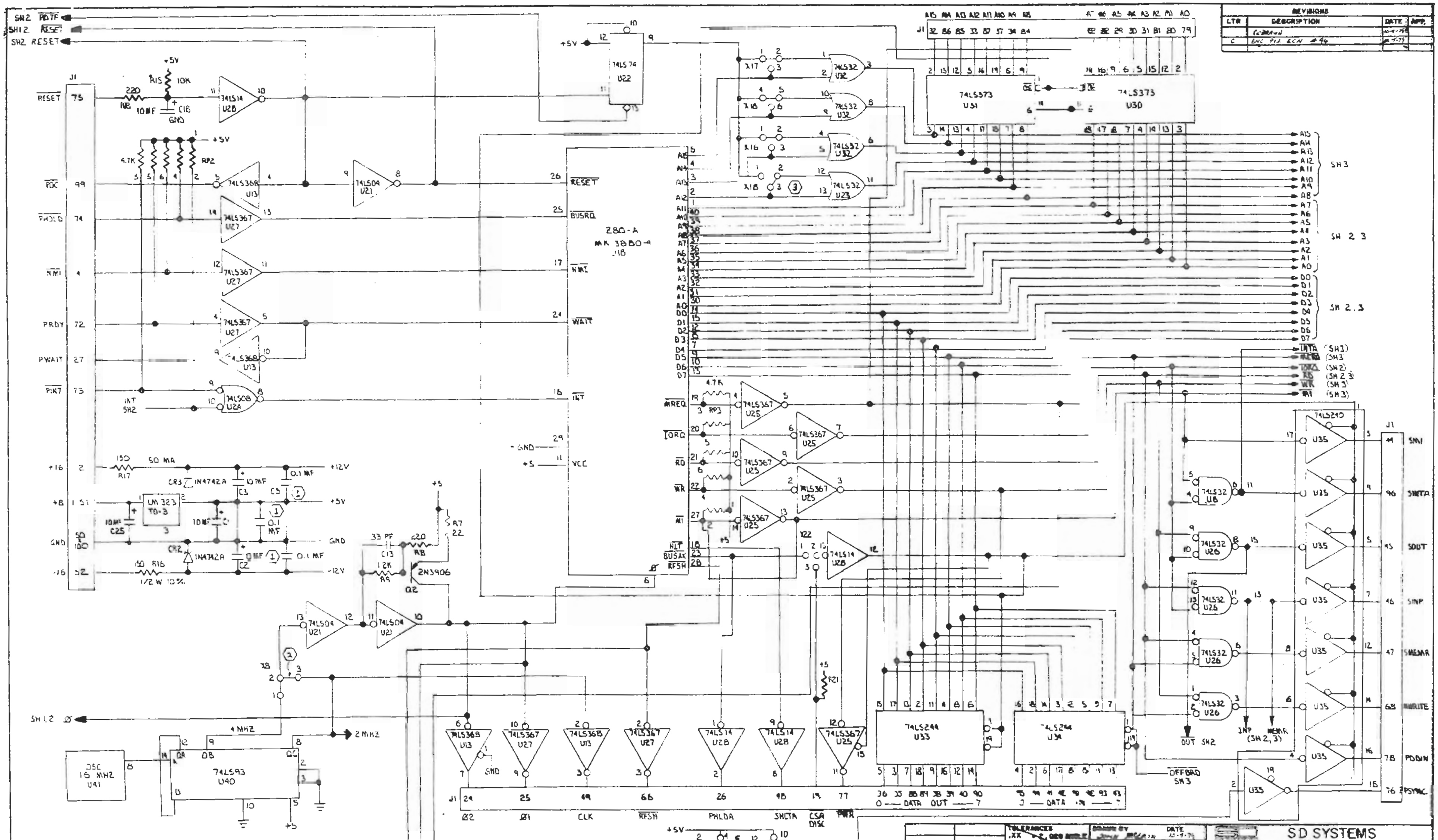
6. Refer to other sections for proper configuration of jumper options and connect jumpers as required.

7. For normal operation with SDOS or COSMOS connect the following using PV jumper clips:

X3	Pins 9-10,11-12,13-14,15-16
X11	Pins 2-3
X13	Pins 2-3
X14	Pins 3-4
X18	Pins 2-3
X20	Pins 1-20

APPENDIX A

SBC-200 SCHEMATIC

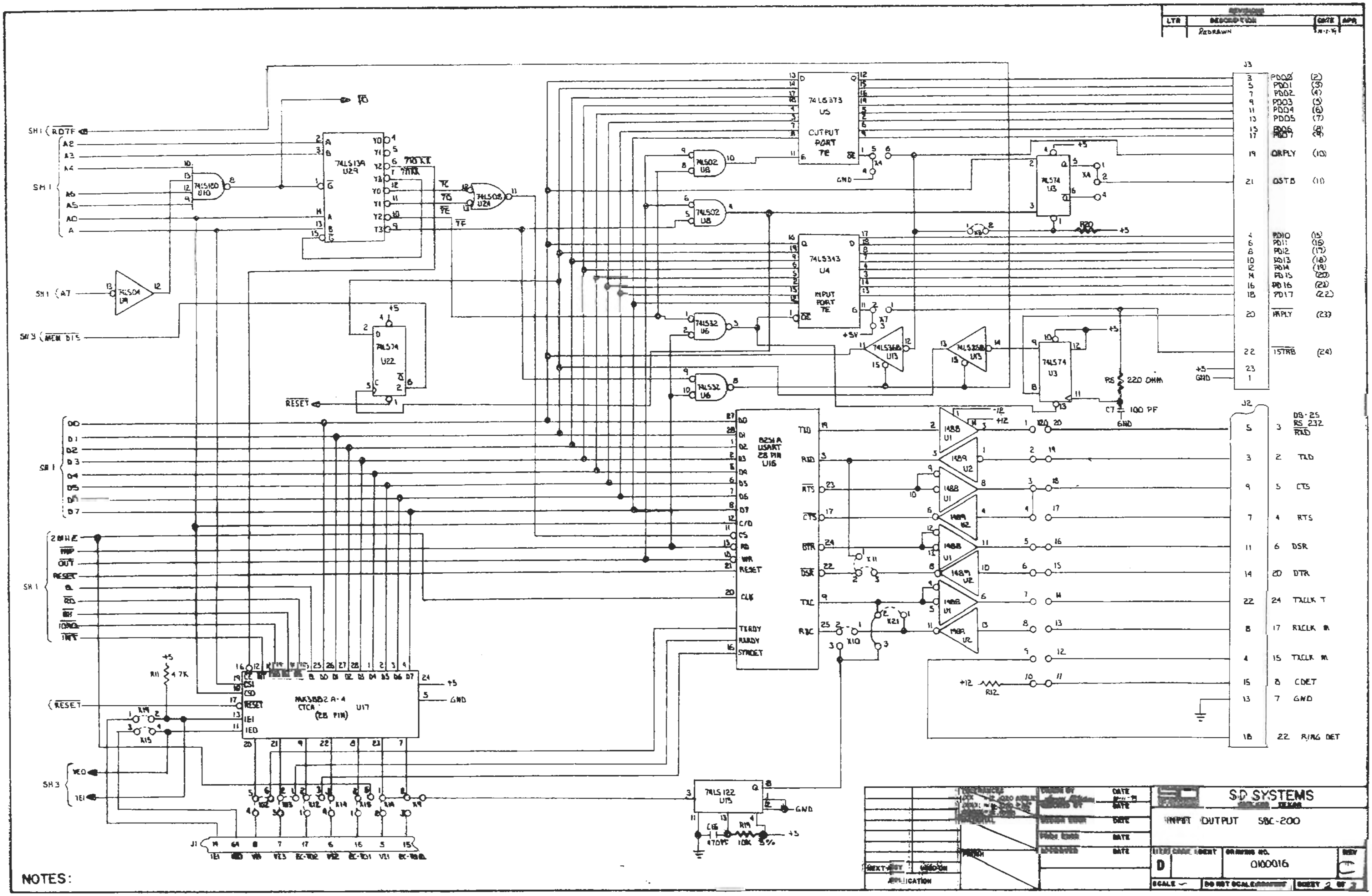


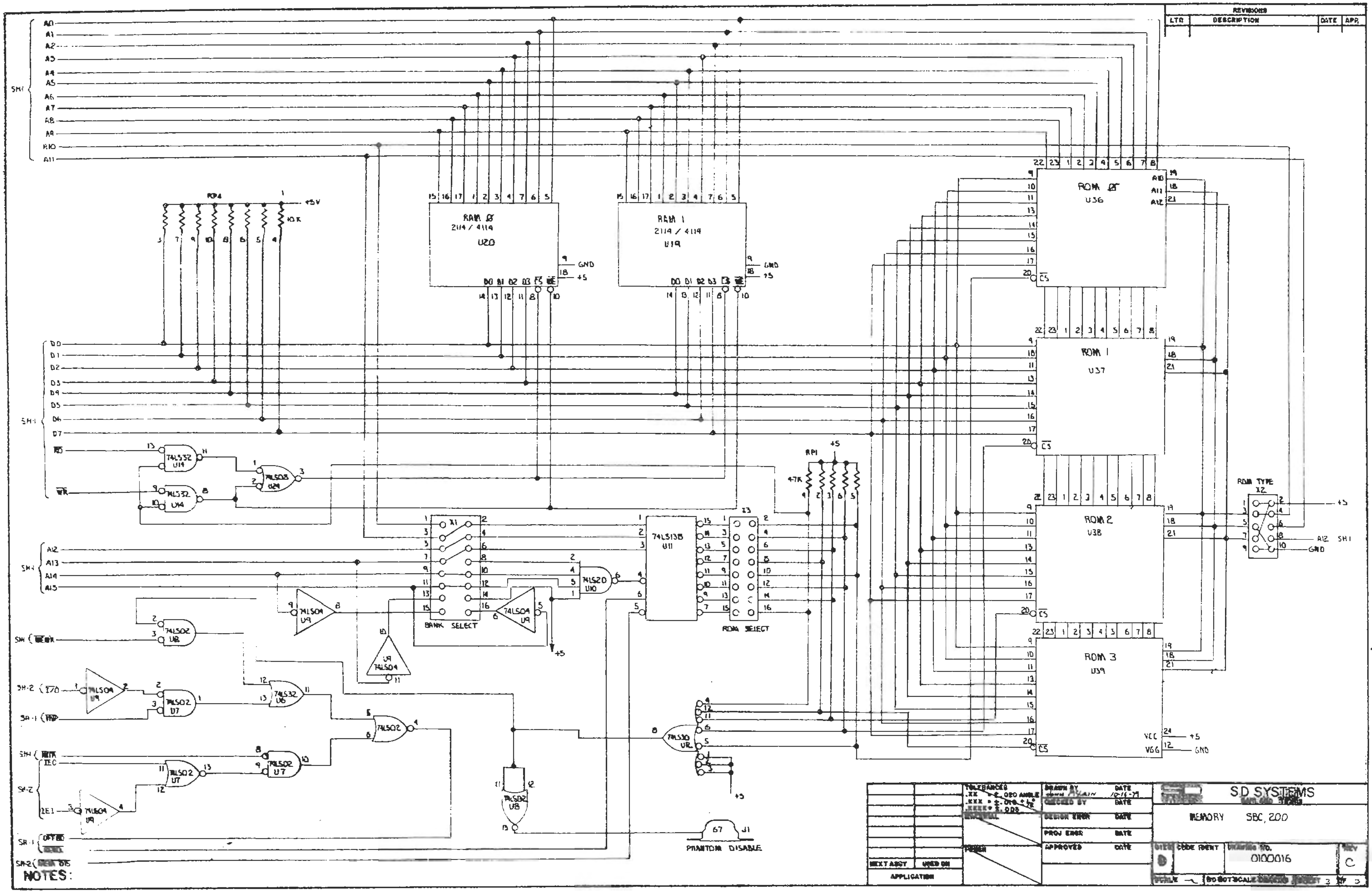
NOTES:

(3) ADD JUMPER FOR SD 200 & 100A

(A) ADD JUMPER FOR 100A
CUT JUMPER 1 TO 2 ON X8

(1) ALL DECOUPLINGS CAPACITORS FROM C4-C6 C8-C12 C17 C19-24 ARE 0.1 MF


SD SYSTEMS
INPUT OUTPUT SBC-200
0100016
D
REDRAWN
74LS373 U5 OUTPUT PORT 7E
74LS373 U4 INPUT PORT 7E
74LS139 U29
74LS30 U10
74LS02 U24
74LS04 U9
74LS74 U22
74LS74 U3
74LS02 U8
74LS32 U6
74LS368 U13
8251A USART 28 PIN U15
MK3882 A-4 CTCA (28 PIN) U17
74LS122 U15
1488 U1
1489 U2
R5 220 OHM
C7 100 PF
R11 4.7K
R12
DB-25 RS 232
RXD
TXD
CTS
RTS
DSR
DTR
TXCLK T
RXCLK R
TXCLK R
CDET
GND
RING DET
J1
J2
J3
RDTF
RESET
MEM DIS
SH1
SH3
NOTES:



RAM Ø 2114 / 4114 U20
RAM 1 2114 / 4114 U19
ROM Ø U36
ROM 1 U37
ROM 2 U38
ROM 3 U39
74LS138 U11
74LS20 U10
74LS30 U12
74LS04 U9
74LS32 U14
74LS08 U24
74LS02 U8
74LS02 U7
74LS32 U6
74LS32 U8
BANK SELECT
ROM SELECT
ROM TYPE X2
RP1 4.7K
RP4 10K
+5V
+5
GND
A12 SH1
PHANTOM DISABLE
J1
SH1
SH-2
SH-1
NOTES:
SD SYSTEMS
MEMORY SBC 200
0100016
C

APPENDIX B

SBC-200 PARTS LIST

SD Systems

P.O. Box 28810 • Dallas, Texas 75228 214-271-4667

BILL OF MATERIALS

Title: SBC-200 SINGLE BOARD COMPUTER	PL No. 0100015	Rev. D
Date Released:	Approved: EAS 8-13-79 CLP	Sheet 2 of 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
1	1	7000016	PC BOARD 0100017		
2	1	7010334	Z 80A CPU MK3880-4 U18		
3	1	7010388	CTC-A MK 3882-4 U17		
4	2	7010321	RAM 2114 U19, 20		
5	1	7010341	USART 8251 U16		
6	1	7080006	16 MHZ CRYSTAL OSCILLATOR Y1		
7	2	7010162	74LS02 U7, 8		
8	2	7010164	74LS04 U9, 21		
9	1	7010166	74LS08 U24		
10	1	7010172	74LS14 U28		
11	1	7010174	74LS20 U10		
12	1	7010180	74LS30 U12		
13	4	7010181	74LS32 U6, 14, 26, 32		
14	3	7010195	74LS74 U3, 22, 23		
15	1	7010213	74LS122 U15		
16	1	7010219	74LS138 U11		
17	1	7010220	74LS139 U29		
18	1	7010260	74LS240 U35		
19	2	7010264	74LS244 U33, 34		
20	2	7010302	74LS367 U25, 27		
21	1	7010303	74LS368 U13		
22	4	7010304	74LS373 U 4, 5, 30, 31		
23	1	7010332	75188/MC1488, U1		
24	1	7010333	75189/MC 1489, U2		

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BILL OF MATERIALS

Title: SBC-200 SINGLE BOARD COMPUTER	PL No. 0100015	Rev. D
Date Released:	Approved: [signature] 8-13-79 CLF	Sheet 3 of 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
25	19	7060002	SOCKET 14 PIN U1,2,3,6,7,8,9,10,12,14,15,21,22,23,24,26,28,32 & 40		
26	5	7060003	SOCKET 16 PIN U27,29,11,13 & 25		
27	2	7060004	SOCKET 18 PIN U20 & 19		
28	7	7060005	SOCKET 20 PIN U4,5,30,31,33,34 & 35		
29	4	7060007	SOCKET 24 PIN U36-U39		
30	2	7060008	SOCKET 28 PIN U16,17		
31	1	7060009	SOCKET 40 PIN U18		
32	1	7160002	VOLTAGE REG 5V 3A LM323 VR1		
33	5	7030009	CAP. 10 MFD 25V C1, C2, C3, C18 & C25		
34	18	7030045	CAP. .1 MFD 50V C4-6, C8-12, C17, C19-24,		
			C26, C14, C15		
35	2	7130072	PCB EJECTORS		
36	1	7030015	CAPACITOR 470 PFD 50V C16		
38	1	7030047	CAPACITOR 33 PFD 50V C13		
39	1	7030049	CAPACITOR 100 PFD 50V C7		
40	1	7010397	RESISTOR SIP 10K 10 PIN RP4		
41	3	7010398	RESISTOR SIP 4.7K 6 PIN RP1,2,3		
42	3	7020057	RESISTOR 220 OHM 1/4 W 10% R6,8,18		
43	2	7020171	RESISTOR 150 OHM 1/2W 10% R16,17		
45	3	7020089	RESISTOR 4.7K 1/4W 10% R11,20,21		
46	1	7020075	RESISTOR 1.2K 1/4W 10% R9		
47	1	7020033	RESISTOR 22 OHM 1/4W 10% R7		

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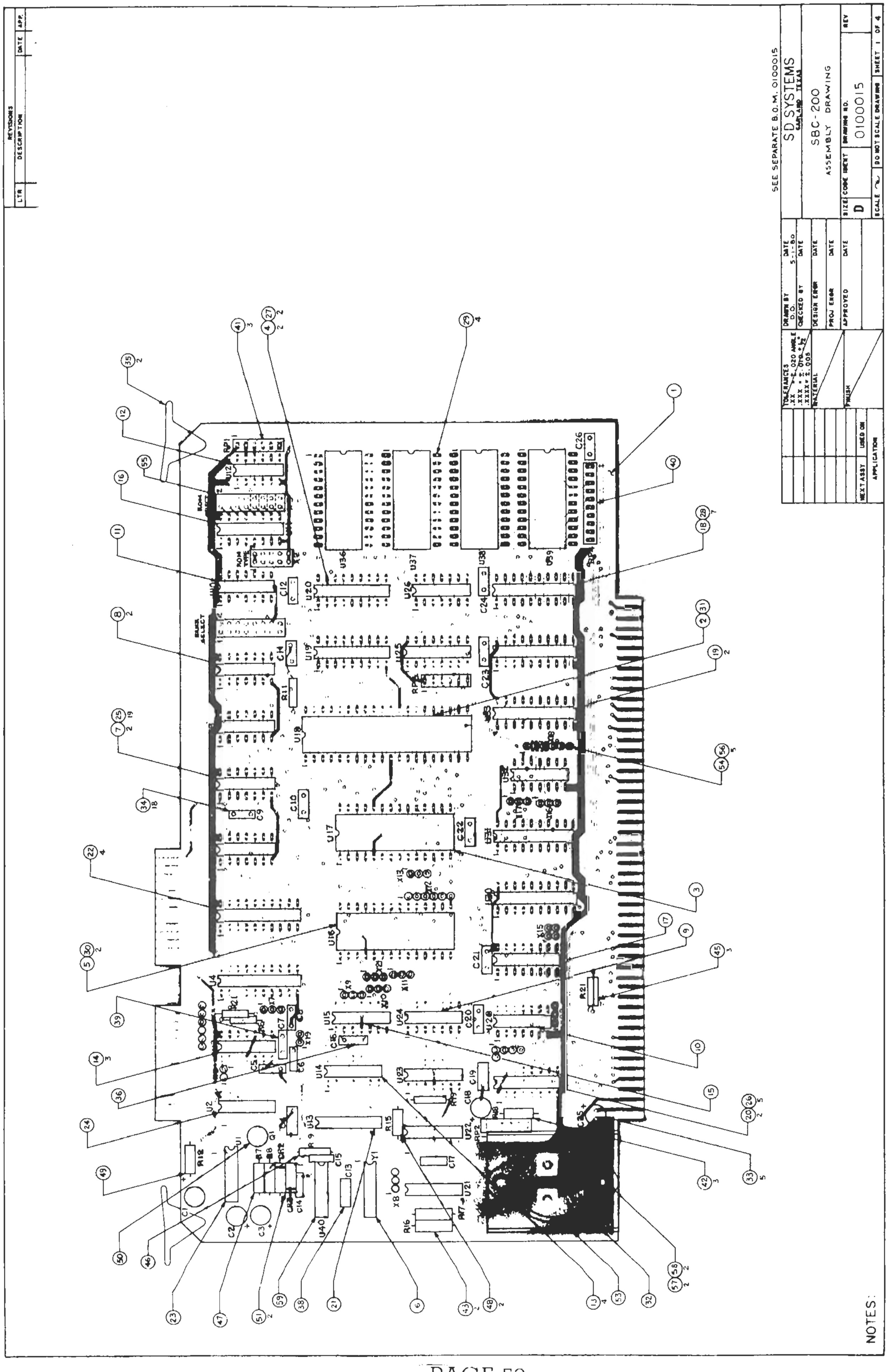
BILL OF MATERIALS

Title: SBC-200 SINGLE BOARD COMPUTER	PL No. 0100015	Rev. D
Date Released:	Approved: ERS 8-13-79	Sheet 4 of 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
48	2	7020097	RESISTOR 10K 1/4W 10% R15, 19		
49	1	7020082	RESISTOR 2.4K 1/4W R12		
50	1	7040006	TRANSISTOR PNP 2N3906 Q1		
51	2	7040004	DIODE ZENER 12V 5% 1N4742A CR2, CR3		
53	1	7130004	HEAT SINK		
54	1	7170002	BERG STRAIGHT HEADER (1×6) X18		
55	1	7170003	BERG STRAIGHT HEADER (2×8) X3		
56	9	7170004	BERG PV JUMPERS		
57	2	7130006	SCREW 6-32 X 3/8 PPH		
58	2	7130007	NUT 6-32		
59	1	7010205	74LS93, U40		
60	2	7170021	BERG STRAIGHT HEADER (1×3) ×11 ×13		
61	1	7170018	BERG STRAIGHT HEADER (1×2) ×20 (1-20)		
62	1	7170012	BERG STRAIGHT HEADER (1×4) ×14		

APPENDIX C

SBC-200 ASSEMBLY DRAWING


SEE SEPARATE B.O.M. 0100015
SD SYSTEMS
GARLAND TEXAS
SBC-200
ASSEMBLY DRAWING
D
0100015
SHEET 1 OF 4
NOTES: