

**16384 x 1 BIT DYNAMIC MOS  
RANDOM ACCESS MEMORY**

**DESCRIPTION** The NEC  $\mu$ PD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

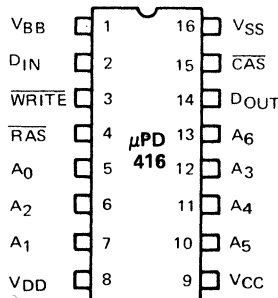
The  $\mu$ PD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

Multiplexed address inputs permit the  $\mu$ PD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

- FEATURES**
- 16384 Words x 1 Bit Organization
  - High Memory Density – 16 Pin Ceramic and Plastic Packages
  - Multiplexed Address Inputs
  - Standard Power Supplies +12V, -5V, +5V
  - Low Power Dissipation; 462 mW Active (MAX), 40 mW Standby (MAX)
  - Output Data Controlled by  $\overline{\text{CAS}}$  and Unlatched at End of Cycle
  - Read-Modify-Write,  $\overline{\text{RAS}}$ -only Refresh, and Page Mode Capability
  - All Inputs TTL Compatible, and Low Capacitance
  - 128 Refresh Cycles
  - 5 Performance Ranges:

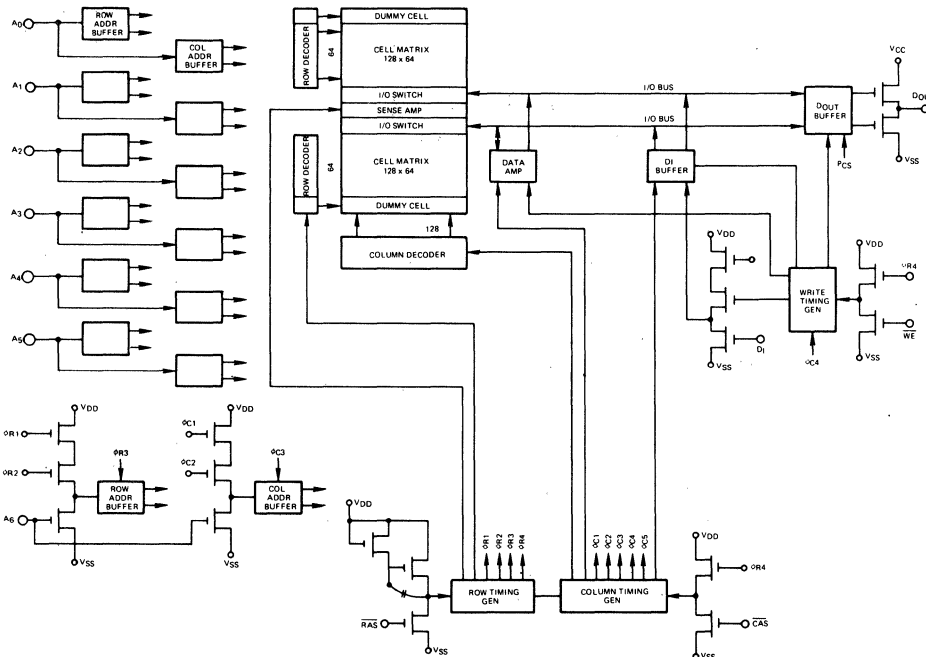
	ACCESS TIME	R/W CYCLE	RMW CYCLE
$\mu$ PD416	300 ns	510 ns	575 ns
$\mu$ PD416-1	250 ns	410 ns	465 ns
$\mu$ PD416-2	200 ns	375 ns	375 ns
$\mu$ PD416-3	150 ns	375 ns	375 ns
$\mu$ PD416-5	120 ns	320 ns	320 ns

**PIN CONFIGURATION**



$\overline{\text{A0-A6}}$	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{DIN}}$	Data In
$\overline{\text{DOUT}}$	Data Out
$\overline{\text{RAS}}$	Row Address Strobe*
$\overline{\text{WRITE}}$	Read/Write
$\overline{\text{VBB}}$	Power (-5V)
$\overline{\text{VCC}}$	Power (+5V)
$\overline{\text{VDD}}$	Power (+12V)
$\overline{\text{VSS}}$	Ground

BLOCK  
DIAGRAM



Operating Temperature .....	0°C to +70°C
Storage Temperature .....	-55°C to +150°C
All Output Voltages ① .....	-0.5 to +20 Volts
All Input Voltages ① .....	-0.5 to +20 Volts
Supply Voltages V <sub>DD</sub> , V <sub>CC</sub> , V <sub>SS</sub> ① .....	-0.5 to +20 Volts
Supply Voltages V <sub>DD</sub> , V <sub>CC</sub> ② .....	-1.0 to +15 Volts
Short Circuit Output Current .....	50 mA
Power Dissipation .....	1 Watt

ABSOLUTE MAXIMUM  
RATINGS\*

- Notes: ① Relative to V<sub>BB</sub>  
 ② Relative to V<sub>SS</sub>

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\*T<sub>a</sub> = 25°C

T<sub>a</sub> = 0°C to 70°C, V<sub>DD</sub> = +12V ± 10%, V<sub>BB</sub> = -5V ± 10%, V<sub>CC</sub> = +5V ± 10%,  
 V<sub>SS</sub> = 0V

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A <sub>0</sub> -A <sub>6</sub> ), D <sub>IN</sub>	C <sub>I1</sub>		4	5	pF	
Input Capacitance RAS, CAS, WRITE	C <sub>I2</sub>		8	10	pF	
Output Capacitance (D <sub>OUT</sub> )	C <sub>O</sub>		5	7	pF	

DC CHARACTERISTICS

T<sub>a</sub> = 0°C to +70°C (1), V<sub>DD</sub> = +12V ± 10%, V<sub>CC</sub> = +5V ± 10%, V<sub>BB</sub> = -5V ± 10%, V<sub>SS</sub> = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V <sub>DD</sub>	10.8	12.0	13.2	V	(2)
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	(2) (3)
Supply Voltage	V <sub>SS</sub>	0	0	0	V	(2)
Supply Voltage	V <sub>BB</sub>	-4.5	-5.0	-5.5	V	(2)
Input High (Logic 1) Voltage, RAS, CAS, WRITE	V <sub>IHC</sub>	2.7		7.0	V	(2)
Input High (Logic 1) Voltage, all inputs except RAS, CAS, WRITE	V <sub>IH</sub>	2.4		7.0	V	(2)
Input Low (Logic 0) Voltage, all inputs	V <sub>IL</sub>	-1.0		0.8	V	(2)
Operating V <sub>DD</sub> Current	I <sub>DD1</sub>			35	mA	RAS, CAS cycling; t <sub>RC</sub> = t <sub>RC</sub> Min. (4)
Standby V <sub>DD</sub> Current	I <sub>DD2</sub>			1.5	mA	RAS = V <sub>IHC</sub> , D <sub>OUT</sub> = High Impedance
Refresh V <sub>DD</sub> Current	All Speeds except μPD416-5	I <sub>DD3</sub>		25	mA	RAS cycling, CAS = V <sub>IHC</sub> ; t <sub>RC</sub> = 375 ns (4)
	μPD416-5	I <sub>DD3</sub>		27	mA	
Page Mode V <sub>DD</sub> Current	I <sub>DD4</sub>			27	mA	RAS = V <sub>IL</sub> , CAS cycling; t <sub>PC</sub> = 225 ns (4)
Operating V <sub>CC</sub> Current	I <sub>CC1</sub>				μA	RAS, CAS cycling; t <sub>RC</sub> = 375 ns (5)
Standby V <sub>CC</sub> Current	I <sub>CC2</sub>	-10		10	μA	RAS = V <sub>IHC</sub> , D <sub>OUT</sub> = High Impedance
Refresh V <sub>CC</sub> Current	I <sub>CC3</sub>	-10		10	μA	RAS cycling, CAS = V <sub>IHC</sub> ; t <sub>RC</sub> = 375 ns
Page Mode V <sub>CC</sub> Current	I <sub>CC4</sub>				μA	RAS = V <sub>IL</sub> , CAS cycling; t <sub>PC</sub> = 225 ns (5)
Operating V <sub>BB</sub> Current	I <sub>BB1</sub>			200	μA	RAS, CAS cycling; t <sub>RC</sub> = 375 ns
Standby V <sub>BB</sub> Current	I <sub>BB2</sub>			100	μA	RAS = V <sub>IHC</sub> , D <sub>OUT</sub> = High Impedance
Refresh V <sub>BB</sub> Current	I <sub>BB3</sub>			200	μA	RAS cycling, CAS = V <sub>IHC</sub> ; t <sub>RC</sub> = 375 ns
Page Mode V <sub>BB</sub> Current	I <sub>BB4</sub>			200	μA	RAS = V <sub>IL</sub> , CAS cycling; t <sub>PC</sub> = 225 ns
Input Leakage (any input)	I <sub>I(L)</sub>	-10		10	μA	V <sub>BB</sub> = -5V, 0V ≤; V <sub>IN</sub> ≤ +7V, all other pins not under test = 0V
Output Leakage	I <sub>O(L)</sub>	-10		10	μA	D <sub>OUT</sub> is disabled, 0V ≤ V <sub>OUT</sub> ≤ +5.5V
Output High Voltage (Logic 1)	V <sub>OH</sub>	2.4			V	I <sub>OUT</sub> = -5 mA (3)
Output Low Voltage (Logic 0)	V <sub>OL</sub>			0.4	V	I <sub>OUT</sub> = 4.2 mA

Notes: (1) T<sub>a</sub> is specified here for operation at frequencies to t<sub>RC</sub> ≥ t<sub>RC</sub> (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

(2) All voltages referenced to V<sub>SS</sub>.

(3) Output voltage will swing from V<sub>SS</sub> to V<sub>CC</sub> when activated with no current loading. For purposes of maintaining data in standby mode, V<sub>CC</sub> may be reduced to V<sub>SS</sub> without affecting refresh operations or data retention. However, the V<sub>OH</sub> (min) specification is not guaranteed in this mode.

(4) I<sub>DD1</sub>, I<sub>DD3</sub>, and I<sub>DD4</sub> depend on cycle rate. See Figures 2, 3 and 4 for I<sub>DD</sub> limits at other cycle rates.

(5) I<sub>CC1</sub> and I<sub>CC4</sub> depend upon output loading. During readout of high level data V<sub>CC</sub> is connected through a low impedance (135Ω typ) to data out. At all other times I<sub>CC</sub> consists of leakage currents only.



T<sub>a</sub> = 0°C to +70°C, V<sub>DD</sub> = +12V ± 10%, V<sub>CC</sub> = +5V ± 10%, V<sub>BB</sub> = -5V ± 10%, V<sub>SS</sub> = 0V

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS	
		μPD416		μPD416-1		μPD416-2		μPD416-3		μPD416-5				
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
Random read or write cycle time	t <sub>RC</sub>	510		410		375		320		320		120	ns	③
Read-write cycle time	t <sub>RWC</sub>	575		465		375		375		320			ns	③
Page mode cycle time	t <sub>PC</sub>	330		275		225		170		160			ns	
Access time from RAS	t <sub>RAC</sub>		300		250		200		150		120		ns	④ ⑥
Access time from CAS	t <sub>CAC</sub>		200		165		135		100		80		ns	⑤ ⑥
Output buffer turn-off delay	t <sub>OFF</sub>	0	80	0	60	0	50	0	40	0	35		ns	⑦
Transition time (rise and fall)	t <sub>T</sub>	3	50	3	50	3	50	3	35	3	35		ns	②
RAS precharge time	t <sub>RP</sub>	200		150		120		100		100			ns	
RAS pulse width	t <sub>RAS</sub>	300	10,000	250	10,000	200	32,000	150	32,000	120	10,000		ns	
RAS hold time	t <sub>RSH</sub>	200		165		135		100		80			ns	
CAS pulse width	t <sub>CAS</sub>	200	10,000	165	10,000	135	10,000	100	10,000	80	10,000		ns	
RAS to CAS delay time	t <sub>RCD</sub>	40	100	35	85	25	65	20	50	15	40		ns	⑧
CAS to RAS precharge time	t <sub>CRP</sub>	-20		-20		-20		-20		0			ns	
Row address set-up time	t <sub>ASR</sub>	0		0		0		0		0			ns	
Row address hold time	t <sub>RAH</sub>	40		35		25		20		15			ns	
Column address set-up time	t <sub>ASC</sub>	-10		-10		-10		-10		-10			ns	
Column address hold time	t <sub>CAH</sub>	90		75		55		45		40			ns	
Column address hold time referenced to RAS	t <sub>AR</sub>	190		160		120		95		80			ns	
Read command set-up time	t <sub>RCS</sub>	0		0		0		0		0			ns	
Read command hold time	t <sub>RCH</sub>	0		0		0		0		0			ns	
Write command hold time	t <sub>WCH</sub>	90		75		55		45		40			ns	
Write command hold time referenced to RAS	t <sub>WCR</sub>	190		160		120		95		80			ns	
Write command pulse width	t <sub>WP</sub>	90		75		55		45		40			ns	
Write command to RAS lead time	t <sub>RWL</sub>	120		85		70		50		50			ns	
Write command to CAS lead time	t <sub>CWL</sub>	120		85		70		50		50			ns	
Data-in set-up time	t <sub>DS</sub>	0		0		0		0		0			ns	⑨
Data-in hold time	t <sub>DH</sub>	90		75		55		45		40			ns	⑨
Data-in hold time referenced to RAS	t <sub>DHR</sub>	190		160		120		95		80			ns	
CAS precharge time (for page mode cycle only)	t <sub>CP</sub>	120		100		80		60		60			ns	
Refresh period	t <sub>REF</sub>		2		2		2		2		2		ms	
WRITE command set-up time	t <sub>WCS</sub>	-20		-20		-20		-20		0			ns	⑩
CAS to WRITE delay	t <sub>CWD</sub>	140		125		95		70		80			ns	⑩
RAS to WRITE delay	t <sub>RWD</sub>	240		200		160		120		120			ns	⑩

- Notes:
- ① AC measurements assume t<sub>T</sub> = 5 ns.
  - ② V<sub>IHC</sub> (min) or V<sub>IH</sub> (min) and V<sub>IL</sub> (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V<sub>IHC</sub> or V<sub>IH</sub> and V<sub>IL</sub>.
  - ③ The specifications for t<sub>RC</sub> (min) and t<sub>RWC</sub> (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C < T<sub>a</sub> < 70°C) is assured.
  - ④ Assumes that t<sub>RCD</sub> < t<sub>RCD</sub> (max). If t<sub>RCD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will increase by the amount that t<sub>RCD</sub> exceeds the values shown.
  - ⑤ Assumes that t<sub>RCD</sub> > t<sub>RCD</sub> (max).
  - ⑥ Measured with a load equivalent to 2 TTL loads and 100 pF.
  - ⑦ t<sub>OFF</sub> (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
  - ⑧ Operation within the t<sub>RCD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RCD</sub> (max) is specified as a reference point only. If t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
  - ⑨ These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
  - ⑩ t<sub>WCS</sub>, t<sub>CWD</sub> and t<sub>RWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t<sub>WCS</sub> = t<sub>WCS</sub> (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) ≥ t<sub>RWD</sub> (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

DERATING CURVES

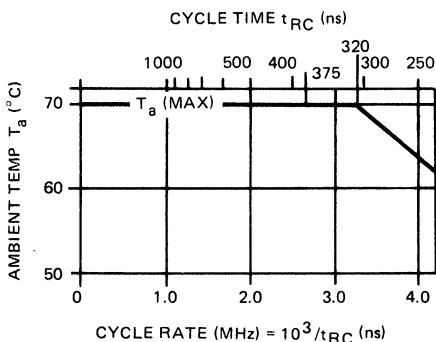


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation.  $T_a$  (max) for operation at cycling rates greater than 2.66 MHz ( $t_{CYC} < 375$  ns) is determined by  $T_a$  (max) [ $^{\circ}$ C] =  $70 - 9.0 \times$  (cycle rate [MHz]  $\times 2.66$ ). For  $\mu$ PD416-5, it is  $T_a$  (max) [ $^{\circ}$ C] =  $70 - 9.0$  (cycle rate [MHz]  $\times 3.125$ ).

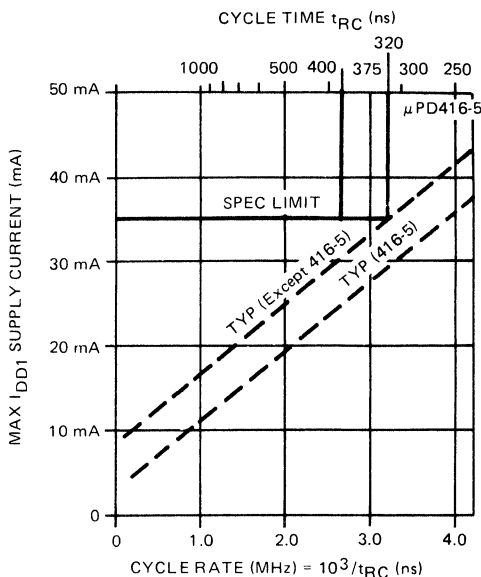


FIGURE 2

Maximum  $I_{DD1}$  versus cycle rate for device operation at extended frequencies.

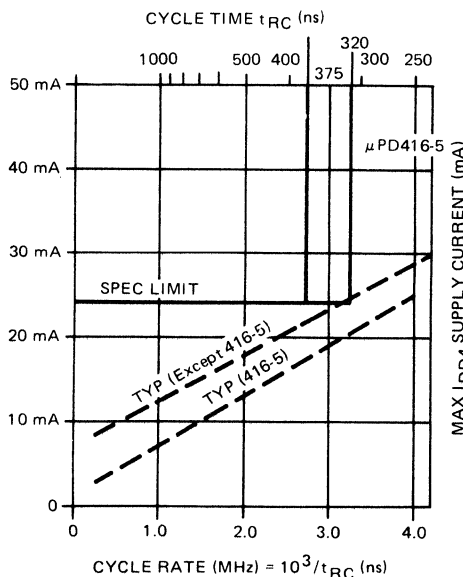


FIGURE 3

Maximum  $I_{DD3}$  versus cycle rate for device operation at extended frequencies.

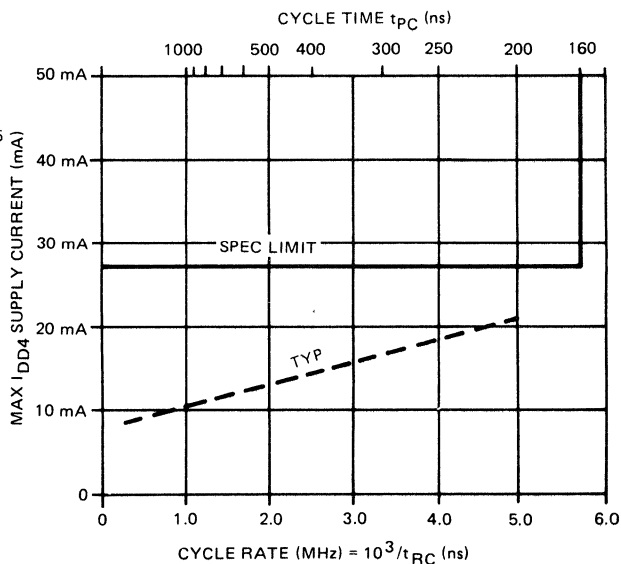
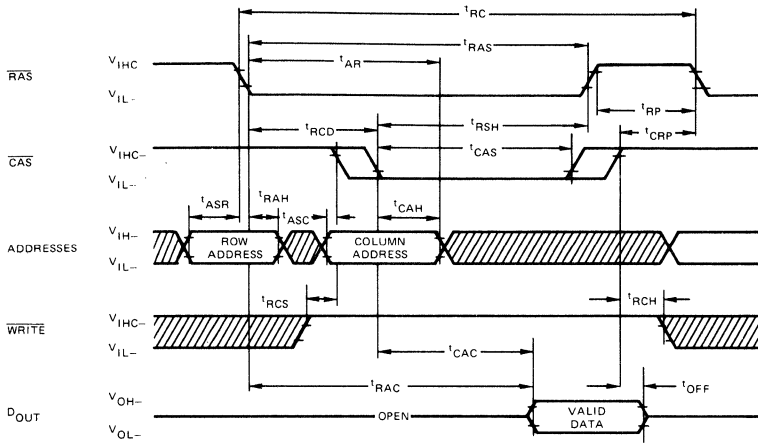


FIGURE 4

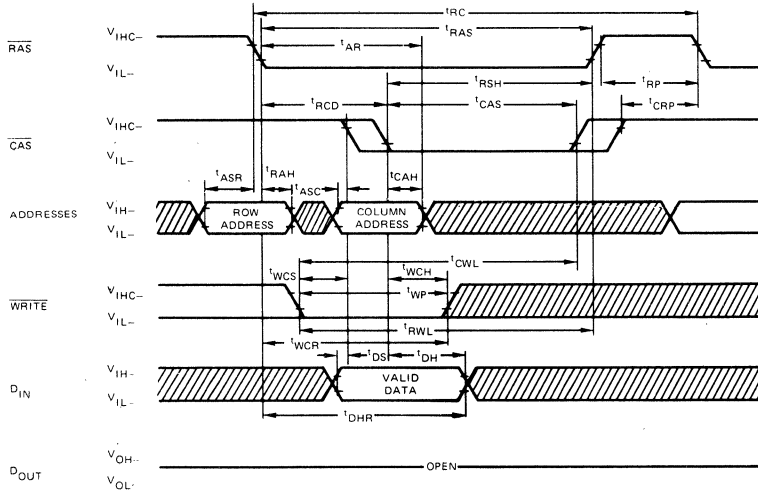
Maximum  $I_{DD4}$  versus cycle rate for device operation in page mode.



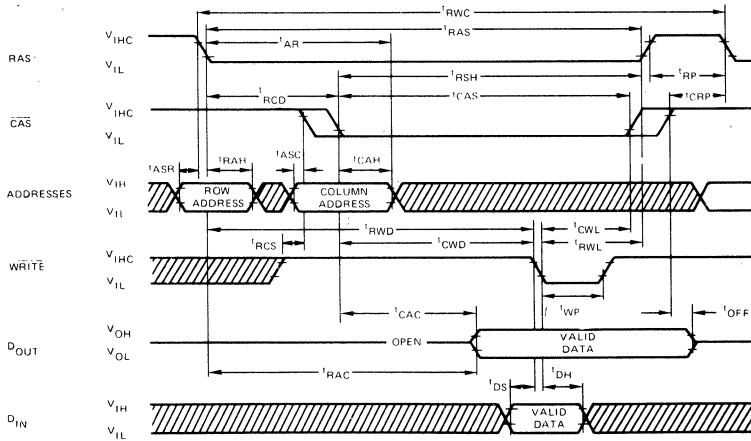
**READ CYCLE**



**WRITE CYCLE**

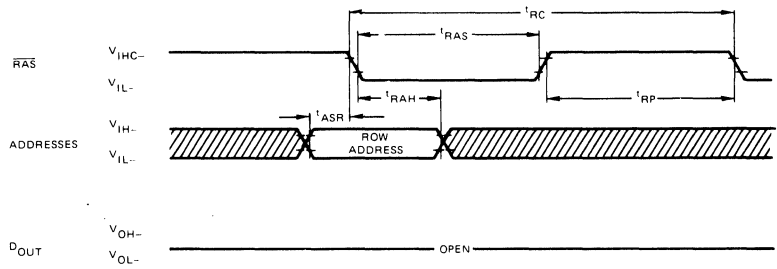


**READ-WRITE/READ-MODIFY-WRITE CYCLE**



TIMING WAVEFORMS  
(CONT.)

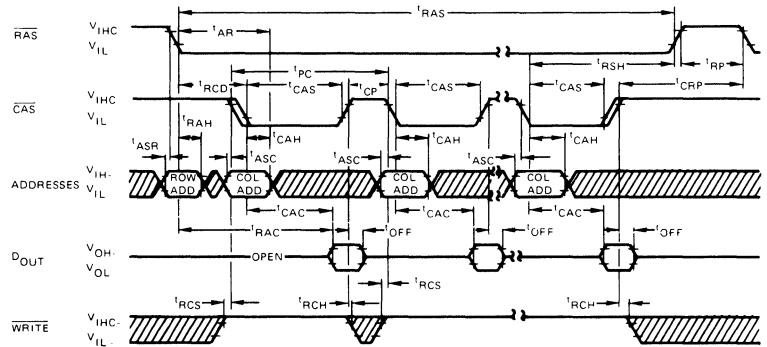
"RAS-ONLY" REFRESH CYCLE



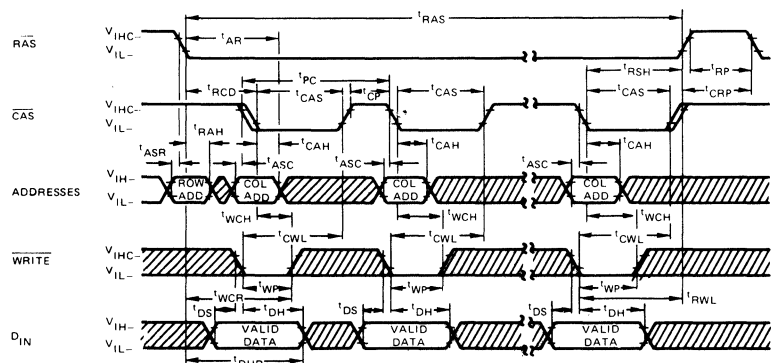
Note  $\overline{\text{CAS}}$ ,  $V_{\text{IH}}$ ,  $\overline{\text{WRITE}}$  = Don't Care

3

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



# $\mu$ PD416

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ( $\overline{\text{RAS}}$ ), and the Column Address Strobe ( $\overline{\text{CAS}}$ ). The 7 bit row address is first applied and  $\overline{\text{RAS}}$  is then brought low. After the  $\overline{\text{RAS}}$  hold time has elapsed, the 7 bit column address is applied and  $\overline{\text{CAS}}$  is brought low. Since the column address is not needed internally until a time of  $t_{\text{CRD MAX}}$  after the row address, this multiplexing operation imposes no penalty on access time as long as  $\overline{\text{CAS}}$  is applied no later than  $t_{\text{CRD MAX}}$ . If this time is exceeded, access time will be defined from  $\overline{\text{CAS}}$  instead of  $\overline{\text{RAS}}$ .

For a write operation, the input data is latched on the chip by the negative going edge of  $\overline{\text{WRITE}}$  or  $\overline{\text{CAS}}$ , whichever occurs later. If  $\overline{\text{WRITE}}$  is active before  $\overline{\text{CAS}}$ , this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that  $\overline{\text{CAS}}$  goes high.

The page mode feature allows the  $\mu$ PD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on  $\overline{\text{RAS}}$  and strobing the new column addresses with  $\overline{\text{CAS}}$ . This eliminates the setup and hold times for the row address resulting in faster operation.

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "RAS only" cycles can be used for simple refreshing operation.

Either  $\overline{\text{RAS}}$  and/or  $\overline{\text{CAS}}$  can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

In order to assure long term reliability,  $V_{\text{BB}}$  should be applied first during power up and removed last during power down.

## ADDRESSING

## DATA I/O

## PAGE MODE

## REFRESH

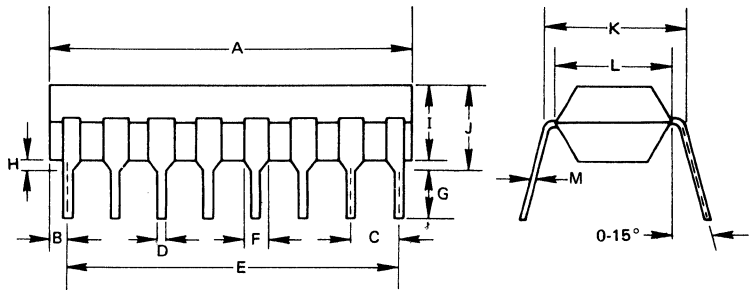
## CHIP SELECTION

## POWER SEQUENCING



# μPD416

## PACKAGE OUTLINE μPD416C

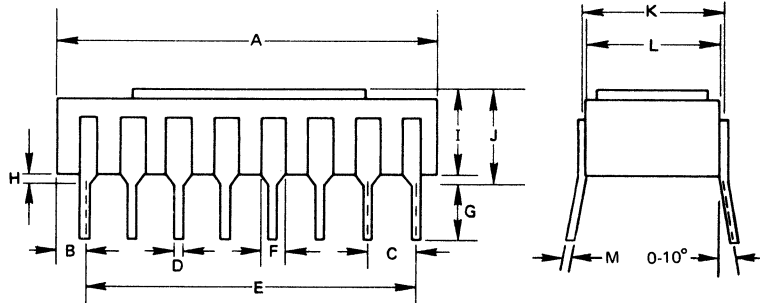


(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	0.25 +0.10 -0.05	0.01

3

## μPD416D



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01