EXPANDORAM III
OPERATIONS MANUAL

SD #7140107
REVISION C
JUNE 8, 1983

SDSYSTEMS
A SYNTECH COMPANY

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1.1 INTRODUCTION

This section provides the purpose, capabilities and limitations of the EXPANDORAM III board.

1.2 GENERAL DESCRIPTION

The EXPANDORAM III board provides a low cost means for expanding Random Access Memory (RAM) capability for computers utilizing the S-100 bus structure. It can use the Z-80 refresh signal and operates at 4 mHz. The latest version (EXPANDORAM III/696) is compatible with S-100 systems complying with the IEEE-696 S-100 specification.

The EXPANDORAM III board is a high performance Dynamic RAM board and uses MOS dynamic memory devices. It may be configured to have a memory capacity of 64K, 128K, 192K or 256K bytes of memory using the MK 4164 (65,536x1 MOS Dynamic RAM).

Additional features:

* EXPANDORAM III/696 version compatible with IEEE-696 S-100 systems.
* Phantom output disable or manual switch selectable output disable.
* Typical power dissipation of 5 watts.
* 4 mHz operation.
* Port addressable board select for multi-user system.

The EXPANDORAM III board is implemented on a single 5.25" x 10.0" x 0.65" Printed Circuit Board. It requires a DC voltage at a level of +7V to +10V. The EXPANDORAM III board is typically interfaced to an SDSystems computer system by connector J-1. Table 1-1 examines the overall specifications for the EXPANDORAM III board. Table 1-2 provides the signal name, direction and description of each connector J1 pin used for EXPANDORAM III.

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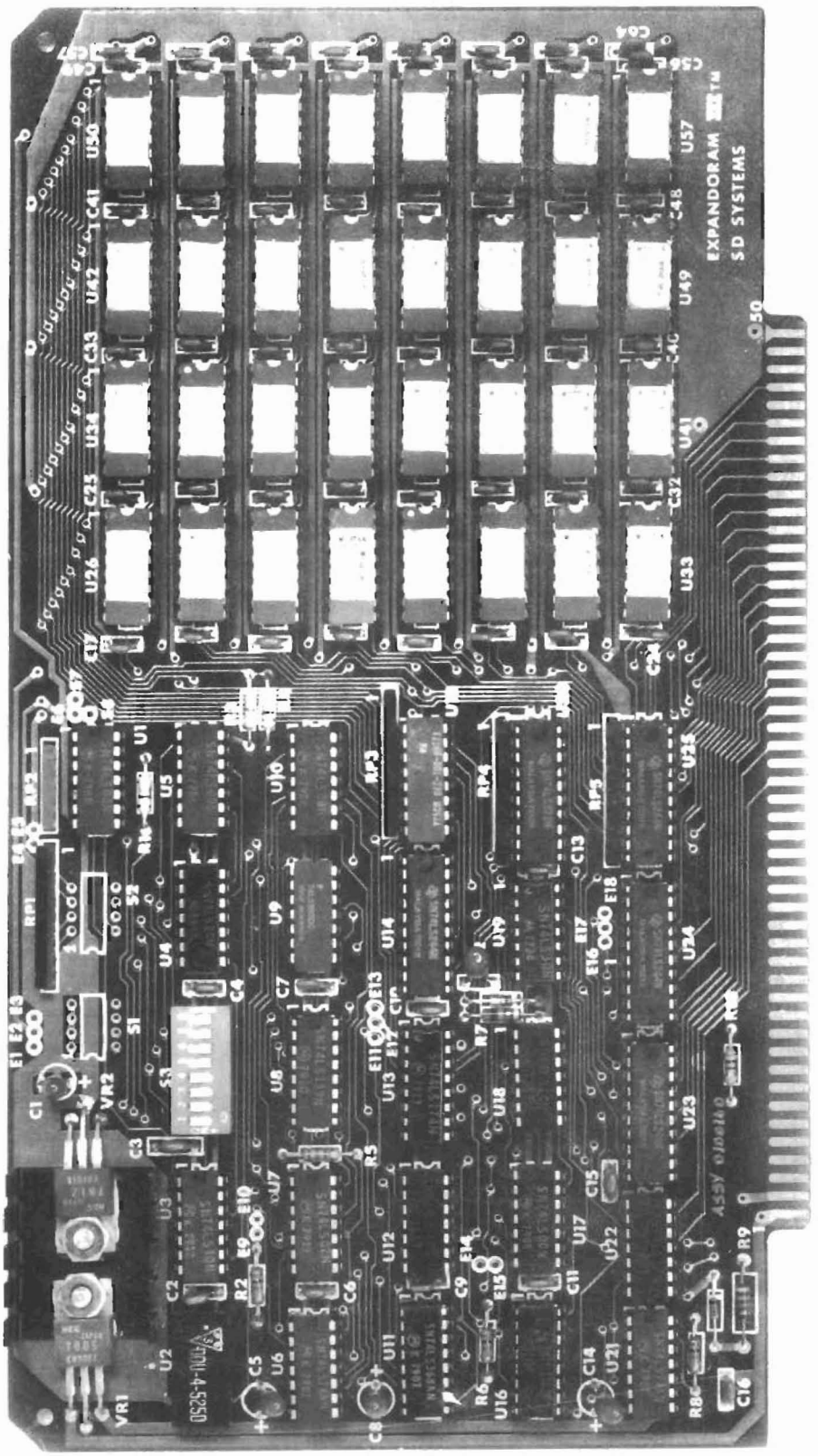


Figure 1-1. EXPANDORAM III BOARD

Table 1-1. EXPANDORAM III SPECIFICATIONS

TOPIC	DATA
Memory Capacity	262,144 bytes
Memory Access	200 ns max.
Memory Cycle	375 ns min.
Interface Levels	TTL Compatible
Power (2 us memory cycle)	+7V to +10V @ 400mA (max)
Physical Dimensions	5.25" x 10.0" x .65"
Operating Temperature	0 degree C to 50 degree C

Table 1-2. EXPANDORAM III CONNECTOR J1 PIN OUT FOR 32K/64K

PIN #	SIGNAL NAME	DIRECTION	DESCRIPTION
1,51	+8V to 10V		Power
24	Ø1 (XRAMIII/696)	Input	Phase 1 clock
25	Ø1 (XRAMIII only)	Input	Phase 1 clock
27	RFU (pWAIT)[1]	Input	Wait
79,80,81, 31,30,29, 82,83	A0-A7	Input	Address bus bits 0-7
84,34,37, 87,33,85, 86,32,	A8-A15	Input	Address bus bits 8-15
36,35,88, 89,38,39, 40,90	D0-0 to D0-7	Input	Data bus in
95,94,41, 42,91,92, 93,43	DI-0 to DI-7	Output	Data bus out
44	sM1	Input	Machine cycle one
47	sMEMR	Input	Memory read
66	NDEF (RFSH)[1]	Input	Refresh (Z80 CPU card)
68	MWRT	Input	Memory write
72	RDY	Output	Ready
78	pDBIN	Input	Data bus in
100,50	GROUND		
45	sOUT	Input	Port Output
99	POC*	Input	Power on Clear
67	PHANTOM*	Input	Phantom Disable

[1] Signal names in parentheses are unique to SDSystems boards and are compatible with IEEE-696 processors.

SECTION II
THEORY OF OPERATION

2.1 INTRODUCTION

This section provides a detailed analysis of the EXPANDORAM III board. It contains:

FUNCTIONAL DESCRIPTION
BOARD PARTS AND DESCRIPTION (Table 2-1)
CIRCUIT ANALYSIS
MEMORY UTILIZATION

2.2 FUNCTIONAL DESCRIPTION

The major functions of the EXPANDORAM III board are shown in figure 2-1. The following functions make up the memory interface: Memory array, memory decode and control, address multiplexer, data buffer, port address decode, and page select.

2.2.1 Memory Array

The memory array consists of up to 32 (16K) dynamic random access memory elements. Each element has a 16,384x1 bit capacity (16K). The 32 (16K) RAMs are organized into four banks of eight RAMs each. The eight RAMs each contribute one bit to an addressable location. The total storage capacity of the EXPANDORAM III is 65,536.

2.2.2 Memory Decode And Control

The memory decode and control circuitry is responsible for generating the timing signals for the memory array, address multiplexer, and data buffer. Timing within the memory decode and control circuitry is generated by a TTL compatible delay line. A PROM is used to select the proper banks according to the address lines, board select switches, and the board select latch. (See Subsection 2.4.1 for more details on PROMs).

2.2.3 Address Multiplexer

The address multiplexer is responsible for taking the address bits from the address bus buffers and multiplexing the proper row and column address into the memory array under control of the memory decode and control circuitry.

2.2.4 Data Buffers

The data buffers isolate the memory array from the data bus controlled by the memory decode and control section.

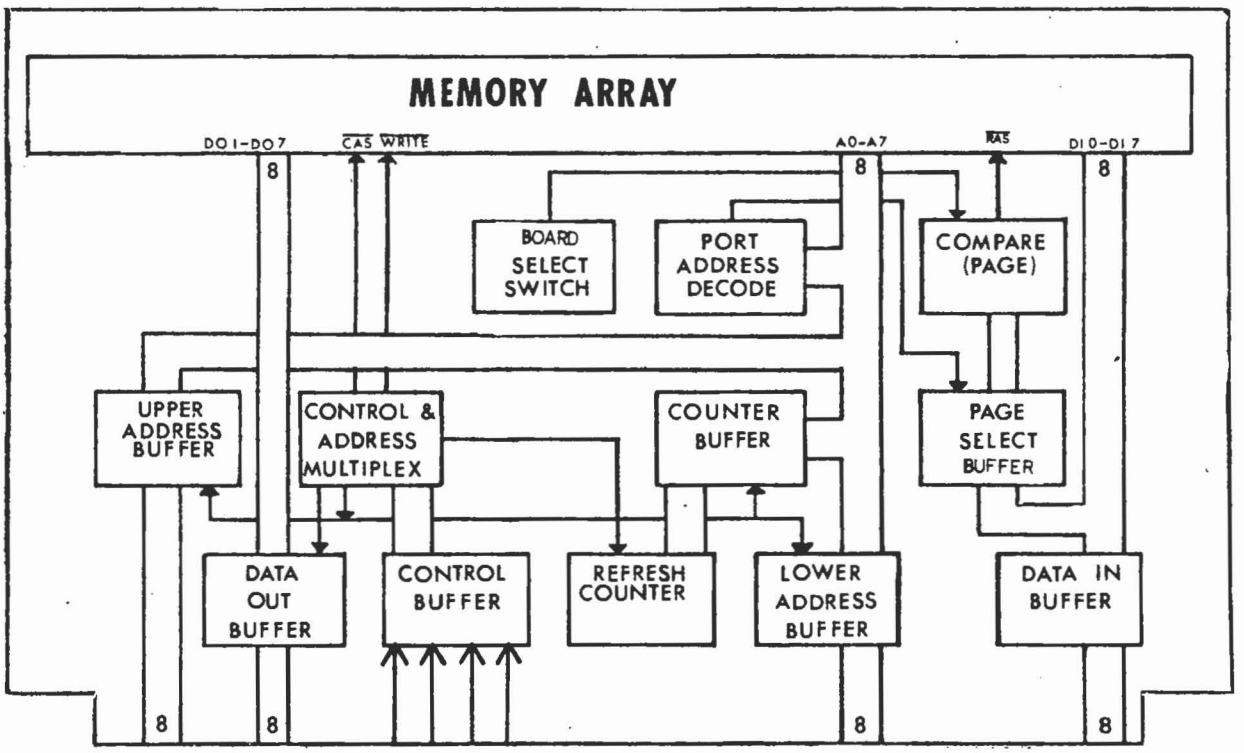


Figure 2-1. EXPANDORAM III BLOCK DIAGRAM

2.2.5 Port Address Decode

The port address decodes port FF and latches the page select data.

2.2.6 Page Select

Page select is performed by a page number latch and decoded by the on-board PROM.

2.3 CIRCUIT ANALYSIS (Reference Schematic Appendix)

Table 2-1 provides a functional description of major EXPANDORAM III board parts. The circuit analysis references parts by designator and is organized as follows: Port decode, phantom, refresh, read, write, wait states, and power.

Table 2-1. EXPANDORAM III BOARD PARTS AND DESCRIPTION

LOCATION	DESCRIPTION
U21	Flip Flop Wait State
U13	Port Input Latch
U19	Port FF Decoder
U8, S3	Board Address Decode Logic (Determine which bank and board are enabled)
U5,U1	Bank Enable Select
U2	Column Address Select (Delay Line)
U16	On-Board Refresh Counter
U9,U14	Refresh Address Buffer
U23	Lower Address Buffer
U24	Upper Address Buffer
U25	Data Input Buffer
U20	Data Output Buffer
4x8 chips per bank	RAM Matrix
VR1	Power Supply Regulators

2.3.1 Port Decode

The lower address buffer (U23) is monitored by a NAND gate (U19). When an address FF (Hex) is present on the lower address lines, the output of U19 becomes true (logic level low) and signal FF* is inverted by U22 pin 8. When Pin 1 of U7 is high (refresh **not** occurring **or** memory cycle **not** occurring), the output of U10 pin 11 conditions U7 pin 11 to monitor the input signal sOUT. sOUT is generated by the system Central Processing Unit (CPU) to indicate a data transfer bus cycle to an output device such as the EXPANDORAM III board. When the CPU has sent sOUT and address FF (Hex) to the EXPANDORAM III board, U7 pin 13 becomes true (logic level

high), latching the data on the BDOX bus onto the outputs of U13. The CPU will have placed the required data pattern on the system DOX bus. Because the data input buffer (U25) is always enabled, whatever data is on the system DOX bus will also appear on the BDOX bus.

The output data pattern latched in U13 provides part of the addressing (A2-A5) required by the bipolar PROM (U8) which outputs the correct RAM bank enable data pattern from programmed PROM memory. PROM address bits A0 and A1 are provided from system address bits A14 and A15 which are buffered and inverted by U18 pins 2 and 12. PROM address bits A6-A8 are derived from switches (S3) which are user selectable. Subsection 2.4 provides more information on switch settings and software partition of system memory.

A successful port decode outputs a RAM bank enable data pattern from the PROM (U8) through the bank enable switches (S3) to the row address strobe circuitry (U5 and U1). Any RAM bank enable line that becomes true (logic level low) from the PROM will also generate a true condition at U4 pin 8. This signal will allow data from the RAM matrix to be latched on the outputs of the data output buffer (U20) during a read process.

2.3.2 Phantom

The phantom signal from the CPU is used to disable all data output from the EXPANDORAM III by causing pin 10 of U3 to be a logic low. The output of U3 pin 8 staying high turns off the tri-state data output buffer (U20). The EXPANDORAM III is provided with a jumper which connects E9 to E10. Removal of the jumper disallows use of phantom by the CPU for turning off the individual EXPANDORAM III board.

2.3.3 Refresh

Refresh is required by Dynamic RAM memory devices to maintain valid data stored in an internal memory cell. The EXPANDORAM III is designed to generate refresh cycles from internal timing circuitry **or** from an external command from the system CPU.

An external refresh command NDEF (RFSH*) (pin 66) is inverted by U12 and inverted again by U7. When the output of U7 pin 10 goes low, the transition of a falling edge triggers the one shot (U58) causing a negative going pulse to be output to pin 4 of the flip-flop U6. The output of U6 pin 5 becomes high, conditioning the NAND gate U1 to allow RAM bank enable to become true for all RAS* signals to the RAM matrix. U7 pin 10 going low also goes to U5, placing a logic level high on the inputs of NAND gate U1, causing the RAS* signals to occur.

At the same time, the U7 pin 10 low signal is inverted by U11 pin 9 which inhibits port decode operations from occurring at U7 pin 3 and conditions the binary counter (U9 pin 1) to increment **after** refresh is completed. The U7 pin 10 low signal also inhibits CAS* from occurring at U10 pin 1 and turns **off** the upper address buffer (U24) at U10 pin 9. The U7 pin 10 low signal also turns **off** the lower address buffer (U23) at U17 pin 1 and turns **on** the refresh counter address buffer (U14). The refresh counter contents are gated onto the RAM address lines and a RAS* only refresh cycle is performed.

If the system, in which the EXPANDORAM III is installed, is inactive, an internal decade counter (U16) will count system clock cycles (Ø1, pin 24) buffered at U22 pin 10. The counter (U16) is loaded by a logic level low at pin 9, generated by any previous read, write, or refresh operation. After 10 system clock cycles, a logic level high is input to U17 pin 10 and the next clock cycle on U17 pin 9 places a logic leves low on pin 10 of flip-flop U6. The flip-flop U6 will set, placing a logic level high on pin 8 of U7. This places a logic level low on U7 pin 10 which performs a refresh identical to the external refresh previously described.

When pin 5 of flip-flop U6 is set during the refresh cycle, a logic level high is placed on pin 1 of the delay line (U2). One hundred nanoseconds later, on pin 4 of the delay line, a logic level high on pin 3 of U14 is inverted, conditioning the clock input pin 11 of flip-flop U6. After an additional 150 nanoseconds, pin 2 of the delay line goes high, which clears flip-flop U6 on pin 1 from NAND gate U10 pin 6. Pin 5 of flip-flop U6 goes low and, 100 nanoseconds later, pin 4 of the delay line (U2) goes low, clocking pin 11 of flip-flop U6 which places a logic level low on pin 9 of U6.

2.3.4 Read

A read process uses many of the same circuits previously described in Subsection 2.3.3, Refresh. After the CPU has stabilized a valid memory address on the address bus, a memory read command sMEMR (pin 47) is inverted and placed on pin 2 of U3. The logic level high from U3 pin 12 clocks a logic level high onto pin 5 of flip-flop U6. The delay line (U2) is sequenced with a high signal appearing on pin 12 in 50 nanoseconds, on pin 4 in 100 nanoseconds, and on pin 2 in 250 nanoseconds.

At the time that flip-flop U6 pin 5 goes high, pin 10 of U7 is also high, since a refresh is **not** being serviced. Pin 10 of U7 being high conditions pin 1 of U17 to output a logic level low on pin 3 to **enable** the lower address buffer (U23). Pin 5 of flip-flop U6 also conditions U1 NAND gates to allow the PROM data pattern to pass through, enabling **one** of the RAS* signal lines to **one** of the RAM banks. The row address strobe (RAS*) is implemented using the lower 8 bits of the system address bus.

Fifty nanoseconds later, pin 12 of U2 goes high which gates a logic level low from U10 pin 8 and **enables** the upper address buffer (U24) and **disables** the lower address buffer (U23).

After another 50 nanoseconds, pin 4 of U2 goes high which generates a column address strobe (CAS*) at pin 3 of U10. The CAS* is implemented using the enabled upper 8 bits of the system address bus. The 50 nanosecond delay allows the upper 8 bits of the address lines to stabilize before CAS* occurs.

When pin 12 of the delay line U2 went high, turning **on** the upper address buffer, the same enaable signal (U10 pin 8) also **enabled** the DIX data output buffer (U20). Since CAS* is still to be processed at this time, the data from the RAM matrix (pin 14) is unstable. The memory data is not latched until 250 nanoseconds later when U10 pin 6 goes low, resetting flip-flop U6 pin 5, which causes pin 12 of the delay line to go low, latching the output data buffer with a logic level low on U20 pin 11.

The data in RAM memory is output from the output data latch (U20) when the CPU inputs a pDBIN command (pin 78) which is inverted and gates a logic level high from pin 4 of U7 which enables a logic level low from pin 8 of U3 which turns **on** the output data buffer (U20) on pin 1.

2.3.5 Write

A write process is almost identical to a read process and uses most of the timing circuits employed by a read process. After the CPU has stabilized a valid memory address on the address bus and a valid data pattern of the DOX data bus, a memory write command, MWRT (pin 68) is inverted by U12 pin 12 and placed on pin 13 of U3. The logic level high from U3 pin 12 clocks a logic level high onto pin 5 of flip-flop U6. The RAS* and CAS* sequencing is then identical to a read cycle previously described except that the **write** command on pin 3 of all RAMs in the RAM matrix is held low by U3 pin 6. The data from the data input buffer (U25) is written into memory. Note that, since the data input buffer is **always enabled** (pins 1 and 19), the CPU has all responsibility for valid data being stabilized on the DOX data bus.

2.3.6 Wait States

When the EXPANDORAM III is used with higher speed CPU boards (4 mHz or greater), a jumper must be installed connecting E14 to E15. The jumper in place allows the CPU bus status signal sM1 (pin 44) to initiate a wait state. The CPU will always make sM1 high when the CPU is executing an OP CODE fetch instruction. A logic level high on pin 44 is inverted which places a logic level low on pin 8 of U12.

The logic level low is clocked through flip-flop U21 pin 5 which enables U11 pin 15 with a logic level low. A logic level low is output from U11 pin 13 to pin 72, RDY command. This output will cause the CPU to execute a wait state. The next clock cycle will pre-set flip-flop U21 with a logic level low from pin 9 which forces pin 5 high. Pin 5 at a logic level high will **disable** U11 pin 13 which returns the RDY command to a logic level high.

In systems configured with earlier SDSystems CPU boards (SBC-200), when the RDɪ command is pulled low, an "ECHO" signal from the CPU is placed on pin 27 of the S-100 bus called pWAIT. This signal input on the EXPANDORAM III board prevents the on-board refresh counter (U16) from being accidentally halted by a POC* command occurring during a wait state. A pWAIT command disables NAND gate U17 pin 12.

2.3.7 Power

Power for logic is derived from an on-board regulator (VR1) and decoupled by a series of capacitors. The S-100 bus provides unregulated +8 VDC on pins 1 and 51 and ground reference on pins 50 and 100.

2.4 MEMORY UTILIZATION

The EXPANDORAM III board has been integrated into computer systems which operate on the following software operating systems:

CP/M
MP/M
COSMOS
OASIS

For the memory on the EXPANDORAM III to be utilized correctly, a Programmable Read Only Memory (PROM) (U8) is installed on each board with a SDSystems program written to optimize the memory partitioning required by the operating systems previously mentioned. Specific switch settings and strapping are also required to allow the EXPANDORAM III to function correctly.

2.4.1 Programmable Read Only Memory

The PROM shipped with the EXPANDORAM III board is designed for operating systems which utilize a 48K memory partition per page. A page of memory is typically reserved for each user in an operating system memory allocation. A page number (0-9) is equivalent to a user number (0-9).

The PROM has 9 address lines (A0-A8) which are divided into three fields: S, P, and A (reference Figure 2-2). The S field address bits A6-A8 are developed from the S3 switch settings which provide the board number and a PROM enable. The P field address bits A2-A5 are developed by the system CPU and latched into U13 during a port decode cycle. The P field is the page or user number. The A field address bits A0-A1 are provided by the system CPU on the two upper system address bits A14-A15. The A field is the RAM bank number.

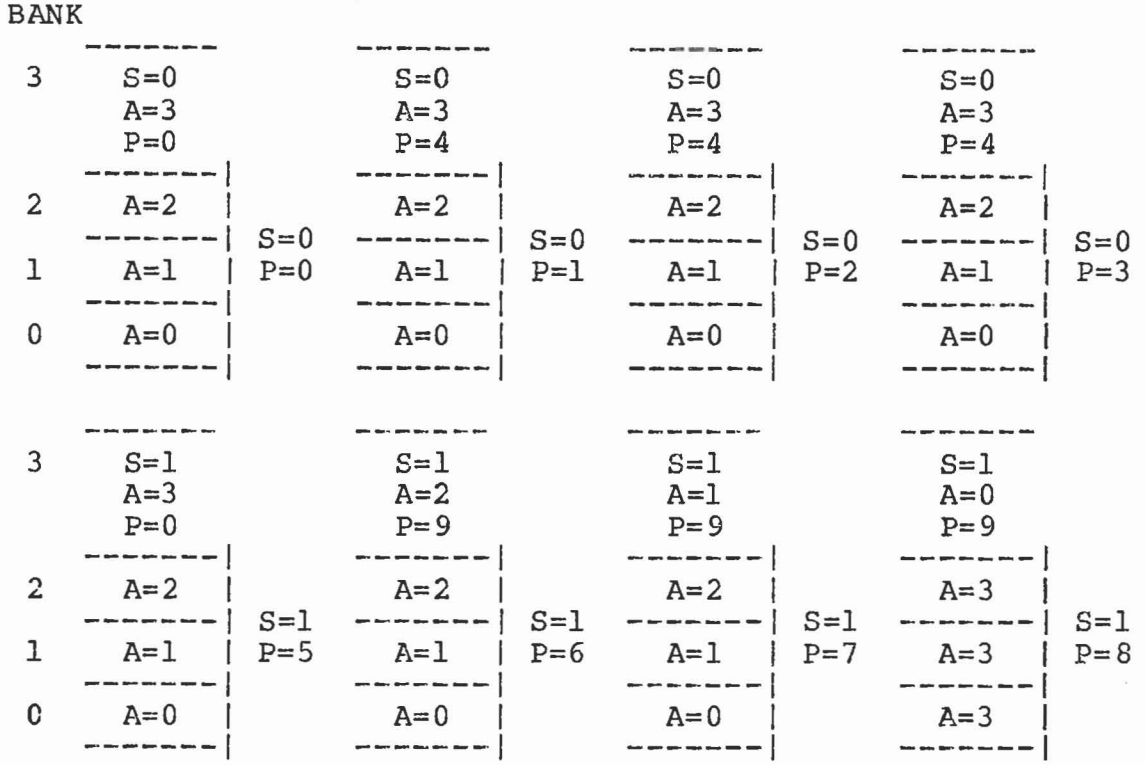
The PROM has 6 output data lines which are utilized in the EXPANDORAM III. Four output data bits are used to enable 1 of the 4 RAM banks in the matrix. The remaining 2 output data bits become address bits A14-A15 in the upper address buffer. Figure 2-2 depicts the page-bank-board map of a typical operating system using 10 48K pages on two EXPANDORAM III boards.

2.4.2 Switch Settings And Strapping

Switch settings information on S3 for the EXPANDORAM III is given in Figure 2-3. Factory setting is all switches **ON.**

Two straps are factory installed: E9-E10 and E14-E15. The straps are required for most SDSystems configurations and software. E9-E10 is used for phantom operation and E14-E15 is used to generate wait states during certain CPU operations.

CP/M, MP/M, COSMOS 48 BOUNDARY SELECTION



OASIS 48 BOUNDARY SELECTION

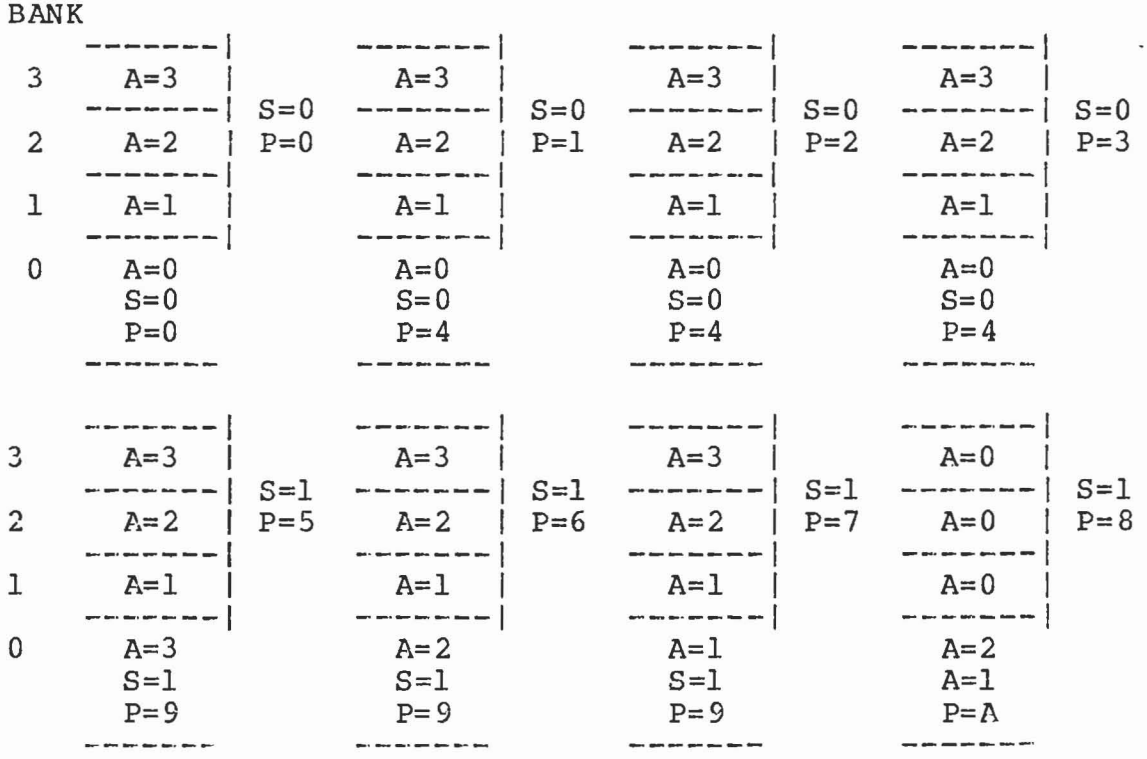


Figure 2-2. PROM PROGRAM AND PAGE MAPPING (Page 1)

			BANK SELECTED	PROM OUTPUT
S (BD)	A8			
(NBR)	A7	0_4	3	7
	A6			
P (USER)	A5	0_3	2	B
(NBR)	A4			
	A3	0_2	1	D
	A2			
A (A15,A14)	A1	0_1	0	E
	A0			

NOTE: P=B,C,D,E,F IS RESERVED.

Figure 2-2. PROM PROGRAM AND PAGE MAPPING (Page 2)

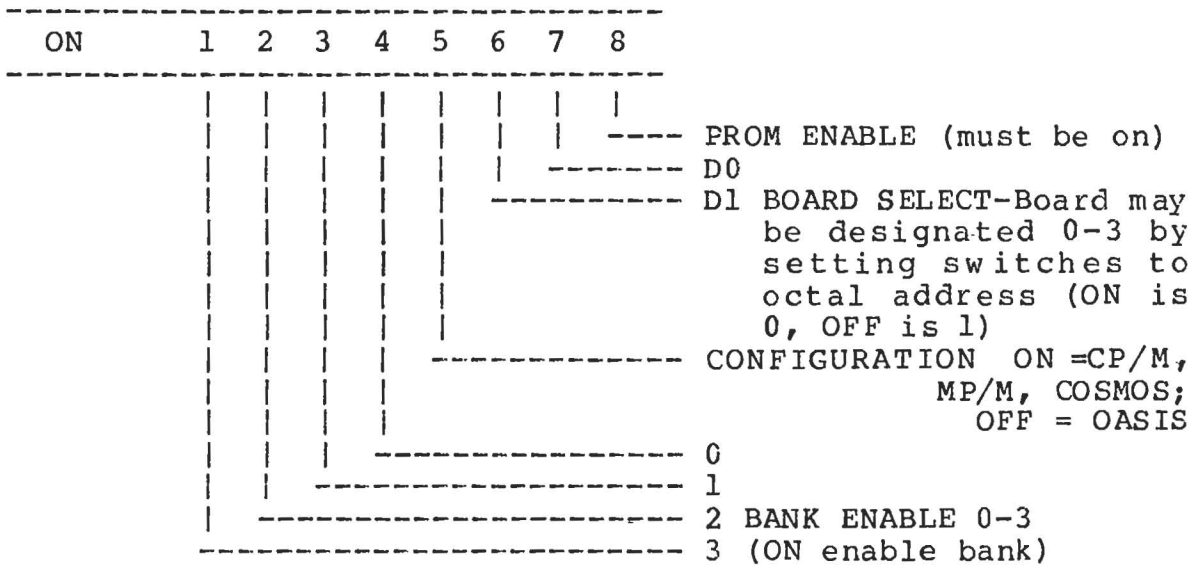


Figure 2-3. EXPANDORAM III S3 SWITCH SETTINGS

2.4.3 EXPANDORAM III In Non-SDSystems Environments

The EXPANDORAM III provides several "jumper" pads for altering the board to operate in a non-SDSystems environment. The board is manufactured with these jumpers connected by etch for operation with SDSystems CPU boards. These jumpers can be modified to operate with other CPU boards.

NOTE: These modifications probably will require modification of both on-board firmware and system software for correct operation.

2.4.3.1 Jumper Pads E22, E23, And E24

These jumpers provide for selection of the S-100 bus pin upon which system clock is received. The board is etched for reception of phase one (Ø1) clock on pin 24 of the S-100 bus. This is an IEEE-696 signal. The jumper can be changed by cutting the etch between E24 and E23 and installing a jumper between E23 and E22. This can allow reception of the system clock on pin 25.

NOTE: This is not supported by IEEE-696. The IEEE-696 signal on pin 25 is pSTVAL.

2.4.3.2 Jumper Pads E25, E26, And E27

The jumper pads E25, E26, and E27 provide for selection between Power On Clear (POC) and RESET as the board reset signal. This allows the capability to reset the EXPANDORAM III by use of the RESET signal. Since RESET is asserted concurrently with POC, this will not affect power up reset.

NOTE: The IEEE-696 signal RESET is to reset bus masters; however, the EXPANDORAM III board is a permanent bus slave. The board is etched to use POC. To use RESET: Cut the etch between E26 and E25 and install a jumper between E26 and E27.

2.4.3.3 Jumpers E16, E17, And E18

The jumper pads E16, E17, and E18 are initially configured such that address line A14 is supplied by the page decode logic (PROM U8 - pin 11). This can be jumpered such that A14 is tied to S-100 bus address line A7. This can be accomplished by cutting the etch between E18 and E17 and attaching a jumper between E17 and E16.

NOTE: This may require firmware modification.

2.4.3.4 Jumpers E19, E20, And E21

The jumper pads E19, E20, and E21 allow the most significant bit of the page decode logic (PROM U8 - pin 16) to be tied to A13* (inverted S-100 bus address line A13). The initial

configuration of these jumpers has this most significant bit of the page decode logic tied to latch U13 - pin 10. The modification can be accomplished by cutting the etch between E19 and E20 and attaching a jumper between E21 and E20.

NOTE: This may require firmware alteration.

2.4.3.5 Jumpers E6, E7, And E8

The jumpers E6, E7, and E8 allow address bit A7 of the on-board RAM matrix to be tied to +5V (high). This allows

selection from 64K to 16K address capability on the multiplexed RAM matrix address lines.

This can be accomplished by cutting the etch between E6 and E7 and attaching a jumper between E6 and E8.

APPENDIX A

SAMPLE MEMORY DIAGNOSTIC SOFTWARE LISTING

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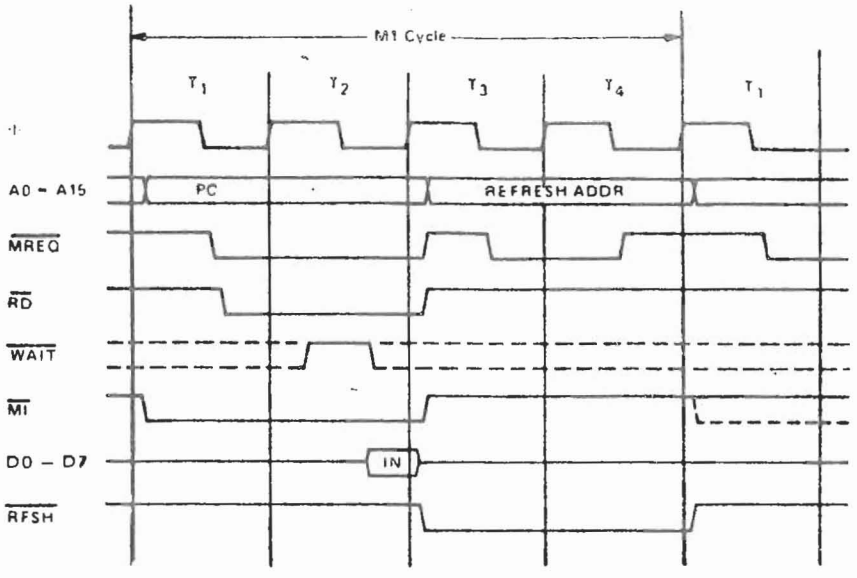
```
ADDR  OBJECT      ST # SOURCE STATEMENT
                  0001 ;TRANSLATED FROM DEC 1976 INTERFACE MAGAZINE
                  0002 ;
                  0003 ;THIS IS A MODIFIED ADDRESS STORAGE TEST WITH
                  0004 ;AN INCREMENTING PATTERN
                  0005 ;
                  0006 ;256 PASSES MUST BE EXECUTED BEFORE THE MEMORY
                  0007 ;IS COMPLETELY TESTED
                  0008 ;
                  0009 ;IF AN ERROR OCCURS, THE PATTERN WILL BE STORED
                  0010 ;AT LOCATION '002C'H AND THE ADDRESS OF THE
                  0011 ;ERROR LOCATION WILL BE STORED AT '002D'H
                  0012 ;AND '002E'H.
                  0013 ;
                  0014 ;THE CONTENTS OF LOCATIONS '000C'H AND '001D'H
                  0015 ;SHOULD BE SELECTED ACCORDING TO THE FOLLOWING
                  0016 ;MEMORY SIZE TESTED
                  0017 ;
                  0018 ;TOP OF MEMORY TO
                  0019 ;BE TESTED                        VALUE OF EPAGE
                  0020 ;
                  0021 ;     4K                               '10'H
                  0022 ;     8K                               '20'H
                  0023 ;    16K                               '40'H
                  0024 ;    32K                               '80'H
                  0025 ;    48K                               'C0'H
                  0026 ;    64K                               'FF'H
                  0027 ;
                  0028 ;THE PROGRAM IS SET UP TO START TESTING AT
                  0029 ;LOCATION '002F'H.  THE STARTING ADDRESS FOR THE
                  0030 ;TEST CAN BE MODIFIED BY CHANGING LOCATIONS
                  0031 ;'0003'H-'0004'H AND '0011'H-'0012'H.
                  0032 ;
                  0033 ;TEST TIME FOR A 16K BY 8 MEMORY IS APPROX. 4 MIN.
                  0034 ;
                  0035 ;        PSECT   ABS
>0000             0036 ;        ORG     0000H
0000  0600        0037 ;        LD      B,0       ;CLEAR B PATRN MODIFIER
                  0038 ;LOAD UP MEMORY
0002  212F00      0039 LOOP:    LD      HL,START  ;GET STARTING ADDR
0005  7D          0040 FILL:    LD      A,L       ;LOW BYTE TO ACCM
0006  AC          0041          XOR     H         ;XOR WITH HIGH BYTE
0007  A8          0042          XOR     B         ;XOR WITH PATTERN
0008  77          0043          LD      (HL),A    ;STORE IN ADDR
0009  23          0044          INC     HL        ;INCREMENT ADDR
000A  7C          0045          LD      A,H       ;LOAD HIGH BYTE OF ADDR
000B  FE10        0046          CP      EPAGE     ;COMPARE WITH STOP ADDR
000D  C20500      0047          JP      NZ,FILL   ;NOT DONE, GO BACK
                  0048 ;READ AND CHECK TEST DATA
0010  212F00      0049          LD      HL,START  ;GET START ADDR
0013  7D          0050 TEST;    LD      A,L       ;LOAD LOW BYTE
0014  AC          0051          XOR     H         ;XOR WITH HIGH BYTE
0015  AB          0052          XOR     B         ;XOR WITH MODIFIER
0016  BE          0053          CP      (HL)      ;COMPARE WITH MEMORY LOC
```

```
0017  C2250000      0054          JP      NZ,EXIT  ;ERROR EXIT
001A  23            0055          INC     HL       ;UPDATE MEMORY ADDR
001B  7C            0056          LD      A,H      ;LOAD HIGH BYTE
001C  FE10          0057          CP      EPAGE    ;COMPARE WITH STOP ADDR
001E  C21300        0058          JP      NZ,TEST  ;LOOP BACK
0021  04            0059          INC     B        ;UPDATE MODIFIER
0022  C30200        0060          JP      LOOP     ;RST WITH NEW MODIFIER
                    0061 ;ERROR EXIT
0025  222D00        0062 EXIT     LD      (BYTE),HL;SAVE ERROR ADDRESS
0028  322C00        0063          LD      (PATRN),A;SAVE BAD PATTERN
002B  76            0064          HALT             ;FLAG OPERATOR
>002C               0065 PATRN:   DEFS    1
>002D               0066 BYTE:    DEFS    2
002F  2F00          0067 START:   DEFW    $
0031  3100          0068          DEFW    $        ;PLACE FOR FIRST ADDR
>0010               0069 EPAGE:   EQU     10H      ;SET UP FOR 4K TEST
                    0070          END
```

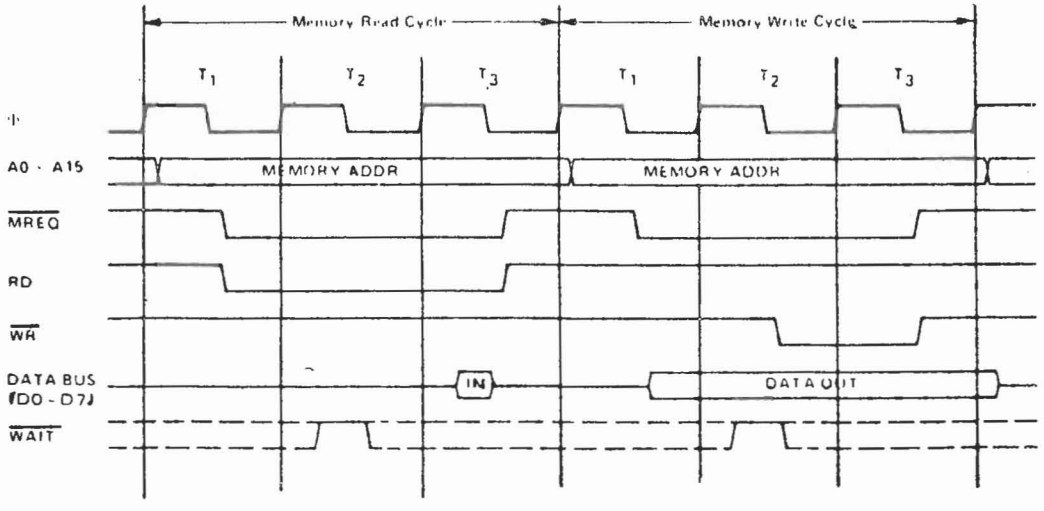
APPENDIX B

TIMING DIAGRAM

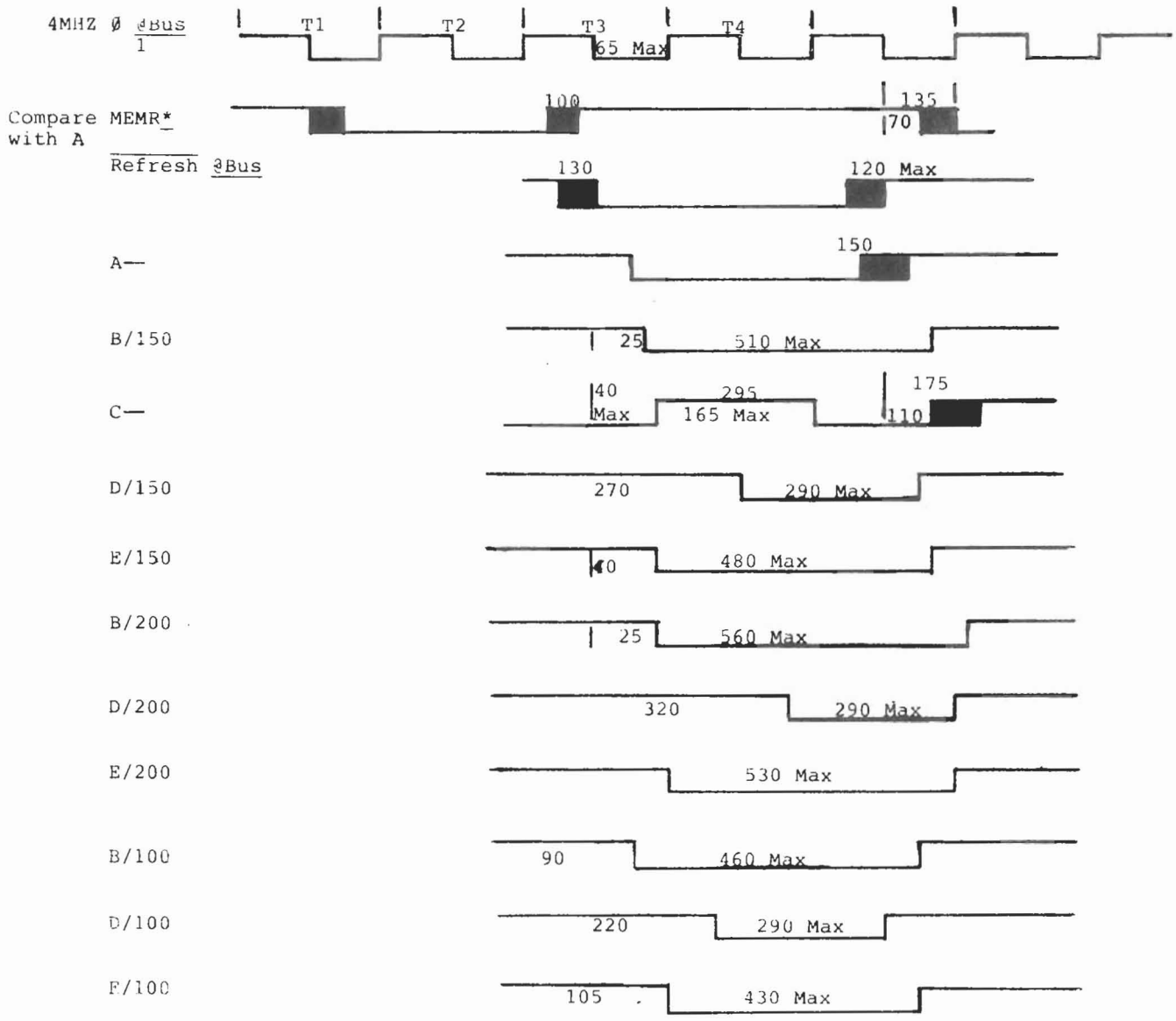
INSTRUCTION OP CODE FETCH



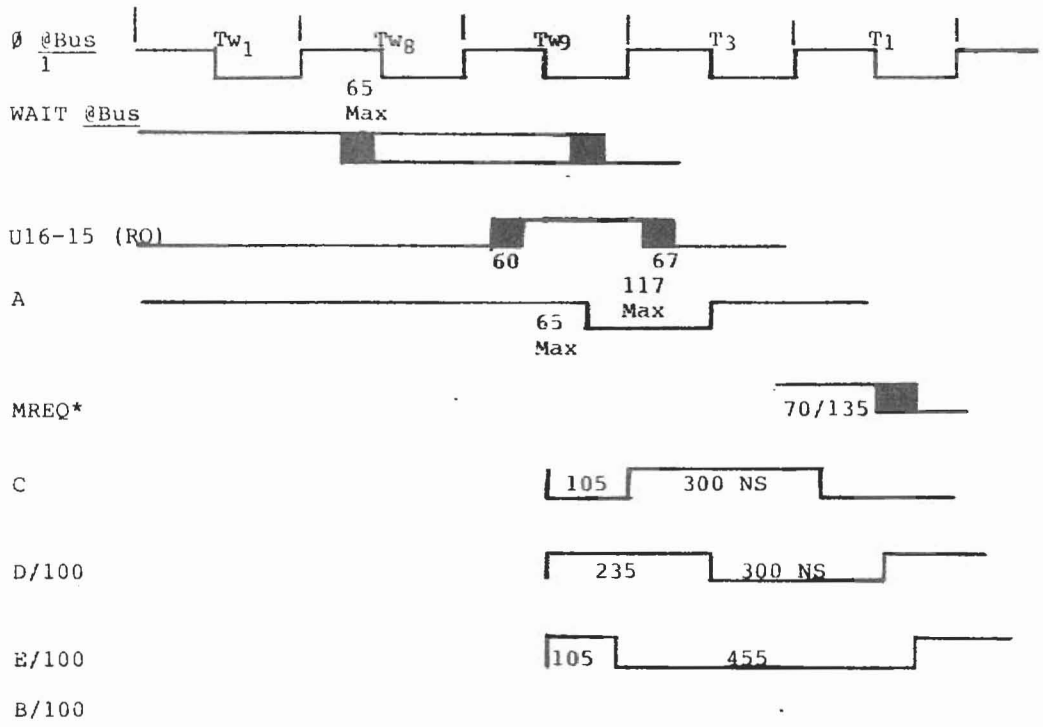
MEMORY READ OR WRITE CYCLES



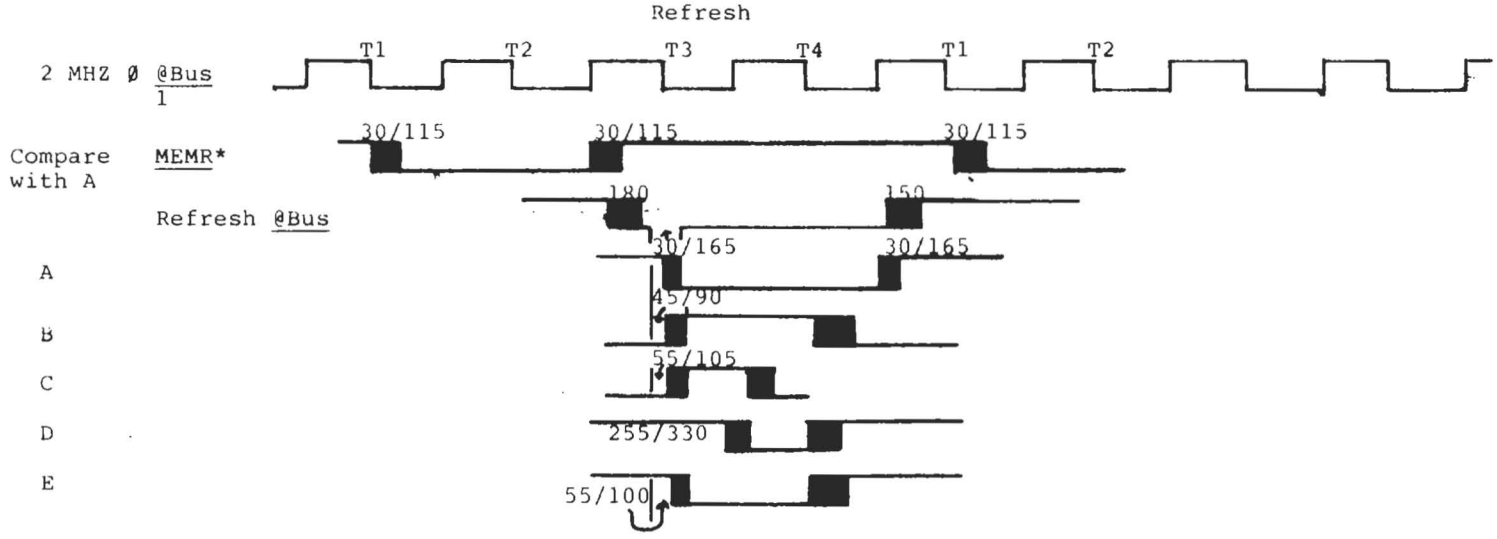
4MHZ M1 REFRESH CYCLE



4 MHZ ONBOARD TIMEOUT REFRESH

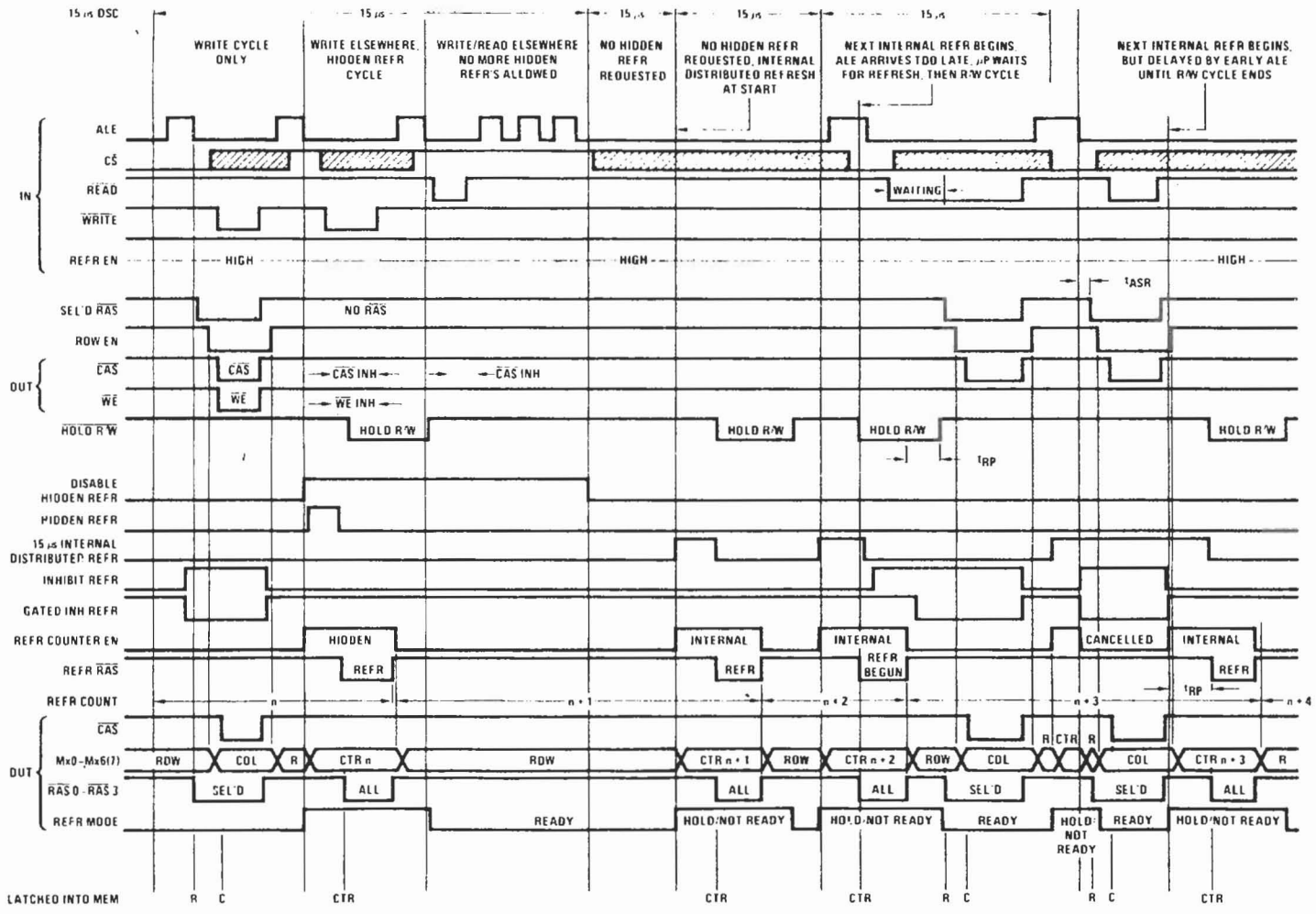


2 MHZ M1 REFRESH CYCLE



ASSUME DELAYS ARE SUCH THAT A SECOND REFRESH CYCLE CAN GET TRIGGERED @ 2MHZ

IN FACT, ANY TIME THE SIGNAL AT B IS SHORT ENOUGH TO RETRIGGER A SECOND REFRESH CYCLE THERE WILL BE ENOUGH TIME TO FINISH THE CYCLE.



Various Combinations of Refresh Timing Waveforms

APPENDIX C

ASSEMBLY DRAWING

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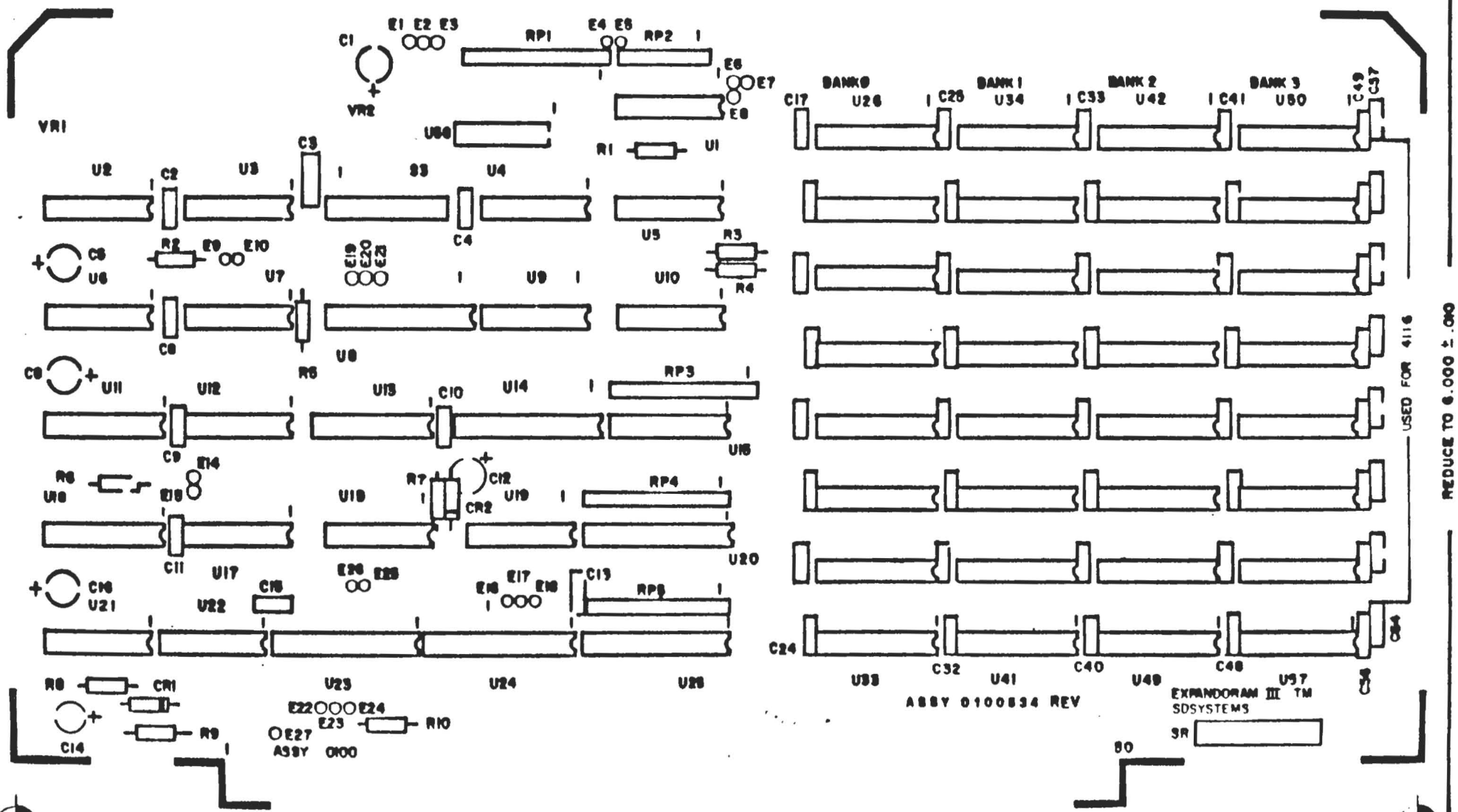
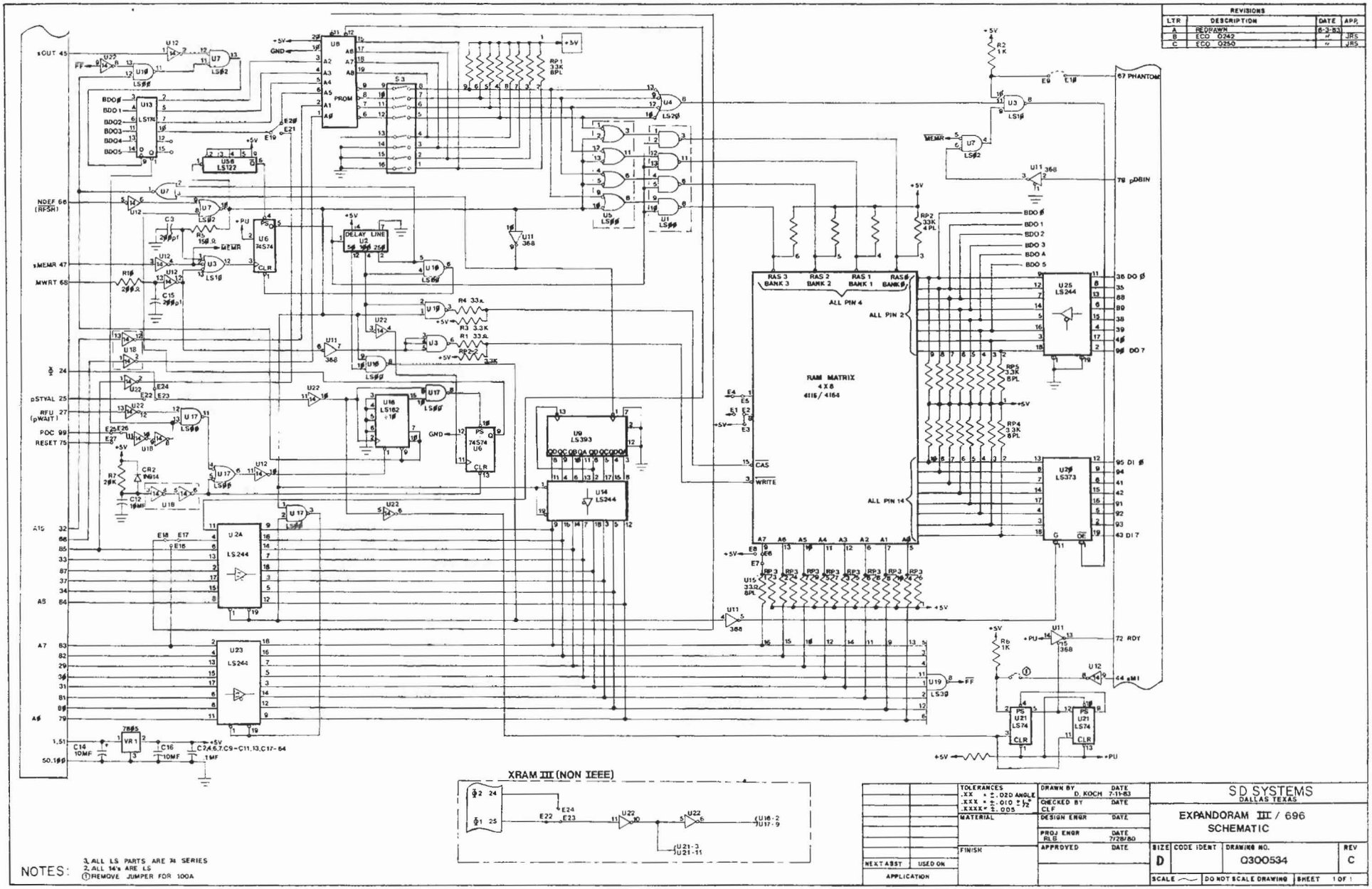
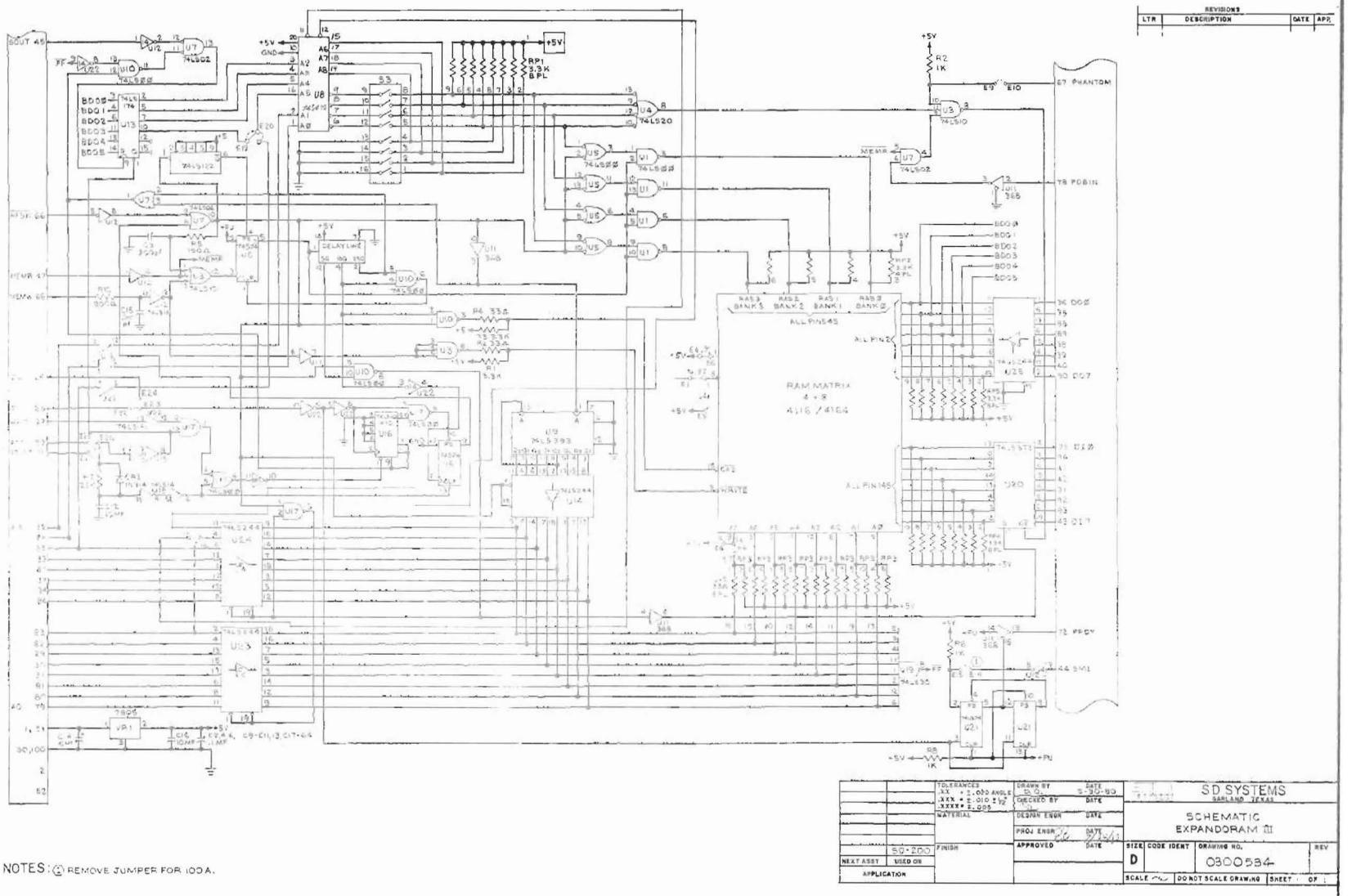

C1
E1 E2 E3
RP1
E4 E5
RP2
E6
E7
E8
VR2
VR1
U36
R1
U1
U2
C2
U3
C3
U4
C4
U5
C5
U6
R2
E9
E10
E19
E20
E21
U7
U9
U10
R3
R4
C8
U8
R5
C9
U11
U12
U13
C10
U14
RP3
U15
R6
E14
E18
U16
R7
C12
CR2
U18
U19
RP4
U20
C11
U17
E26
E25
E17
E16
C13
C16
U21
U22
C15
RP5
R8
CR1
U23
U24
U25
E22
E24
E23
R10
E27
R9
C14
ASSY 0100
BANK0
U26
C17
BANK 1
U34
C25
BANK 2
U42
C33
BANK 3
U50
C41
C49
C37
C24
U33
C32
U41
C40
U49
C48
U57
ASSY 0100534 REV
EXPANDORAM III TM
SDSYSTEMS
SR
80
USED FOR 4116
REDUCE TO 6.000 ± .010
REDUCE TO 10.000 ± .010


REVISIONS
LTR | DESCRIPTION | DATE | APP.
A | REDRAWN | 6-3-83 |
B | ECO 0242 | " | JRS
C | ECO 0250 | " | JRS
XRAM III (NON IEEE)
RAM MATRIX 4 X 8 4115 / 4164
RAS 3 BANK 3
RAS 2 BANK 2
RAS 1 BANK 1
RAS 0 BANK 0
ALL PIN 4
ALL PIN 2
ALL PIN 14
CAS
WRITE
67 PHANTOM
78 pDBIN
72 RDY
44 sM1
NOTES:
1. ALL LS PARTS ARE 74 SERIES
2. ALL 14's ARE LS
(1) REMOVE JUMPER FOR 100A
SD SYSTEMS
DALLAS TEXAS
EXPANDORAM III / 696
SCHEMATIC
DRAWN BY D. KOCH 7-11-83
CHECKED BY CLF
DESIGN ENGR
PROJ ENGR RLE 7/28/80
APPROVED
SIZE D
DRAWING NO. 0300534
REV C
SCALE
DO NOT SCALE DRAWING
SHEET 1 OF 1



NOTES: ① REMOVE JUMPER FOR 100 A.

APPENDIX D

SCHEMATIC

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APPENDIX E

PARTS LIST FOR EXPANDORAM III

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QTY REQD	DESCRIPTION	PART/SUB NUMBER	DESIGNATION
1	EXPANDORAM III PC BOARD	7000028	
4	IC, 74LS00	7010160	U1, U5, U10, U17
1	IC, 74LS02	7010162	U7
1	IC, 74LS10	7010168	U3
3	IC, 74LS14	7010172	U12, U18, U22
1	IC, 74LS20	7010174	U4
1	IC, 74LS30	7010180	U19
2	IC, 74LS74	7010195	U6, U21
1	IC, 74LS162	7010232	U16
1	IC, 74LS174	7010241	U13
4	IC, 74LS244	7010264	U14, U23-U25
1	IC, 74LS368	7010303	U11
1	IC, 74LS373	7010304	U20
1	IC, 74LS393	7010312	U9
36	SOCKET 16 PIN 300 ML	7060003	
6	SOCKET 20 PIN 300 ML	7060005	
47	CAP .1 UF 50 V	7030045	C2, C4, C6, C9-C11, C13, C17-C56
2	CAP 200 PF 50 V 20%	7030043	C3, C15
2	RES 33 OHM 1/4W 5%	7020037	R1, R4
1	RES 200 OHM 1/4W 5%	7020056	R10
3	RES 1K OHM 1/4W 5% CC	7020073	R2, R6, R8
1	IC, 33 OHM 16 PIN RES DIP	7010346	U15
1	IC, 3.3K 6 PIN RES SIP	7010344	RP2
4	IC, 3.3K 10 PIN RES SIP	7010345	RP1, RP3-RP5
1	IC, 74LS122	7010213	U58
1	IC, DDU-4-5250 DELAY LINE	7010366	U2
1	8 POSITION DIP SWITCH	7050002	S3
1	HEATSINK TMH 6106-13	7130003	
1	6-32x3/8 PPH SCREW	7130006	
1	7805-LM 340T-5.0	7160001	VR1
2	PCB EJECTORS	7130072	
1	RES 20K OHM 1/4W	7020104	R7
1	DIODE IN914.1N4148	7040001	CR2
1	RES 150 OHM 1/4W 5%	7020053	R5
1	RES 3.3K OHM 1/4W 5%	7020085	R3
3	65474 BERG PV JUMPER	7170004	
2	BERG 1x2 STR .230 PIN TIN	7170018	E9-E10, E14-E15
3	CAP 10 MF 16 V TANT	7030009	C12, C14, C16
1	COSMOS-48K PROM	7010479	U8
32	4164 RAM	7010422	U26-U57

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